

# ZHG SYSTEM DIAGRAM

**PCB STACK UP**

LAYER 1 : TOP  
LAYER 2 : GND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : VCC  
LAYER 6 : BOT

EDP@ -----> eDP panel  
LVDS@ -----> LVDS panel  
HDT@ -----> HDT fucntion  
3G@ -----> 3G function  
U2@ -----> USB2.0 only  
U3@ -----> USB3.0 function  
885S@ -----> EC885S  
885L@ -----> EC885L

**CHARGER (BQ24707A)** PAGE 21

**AMD CPU CORE (OZ8380)** PAGE 23 *CPU*

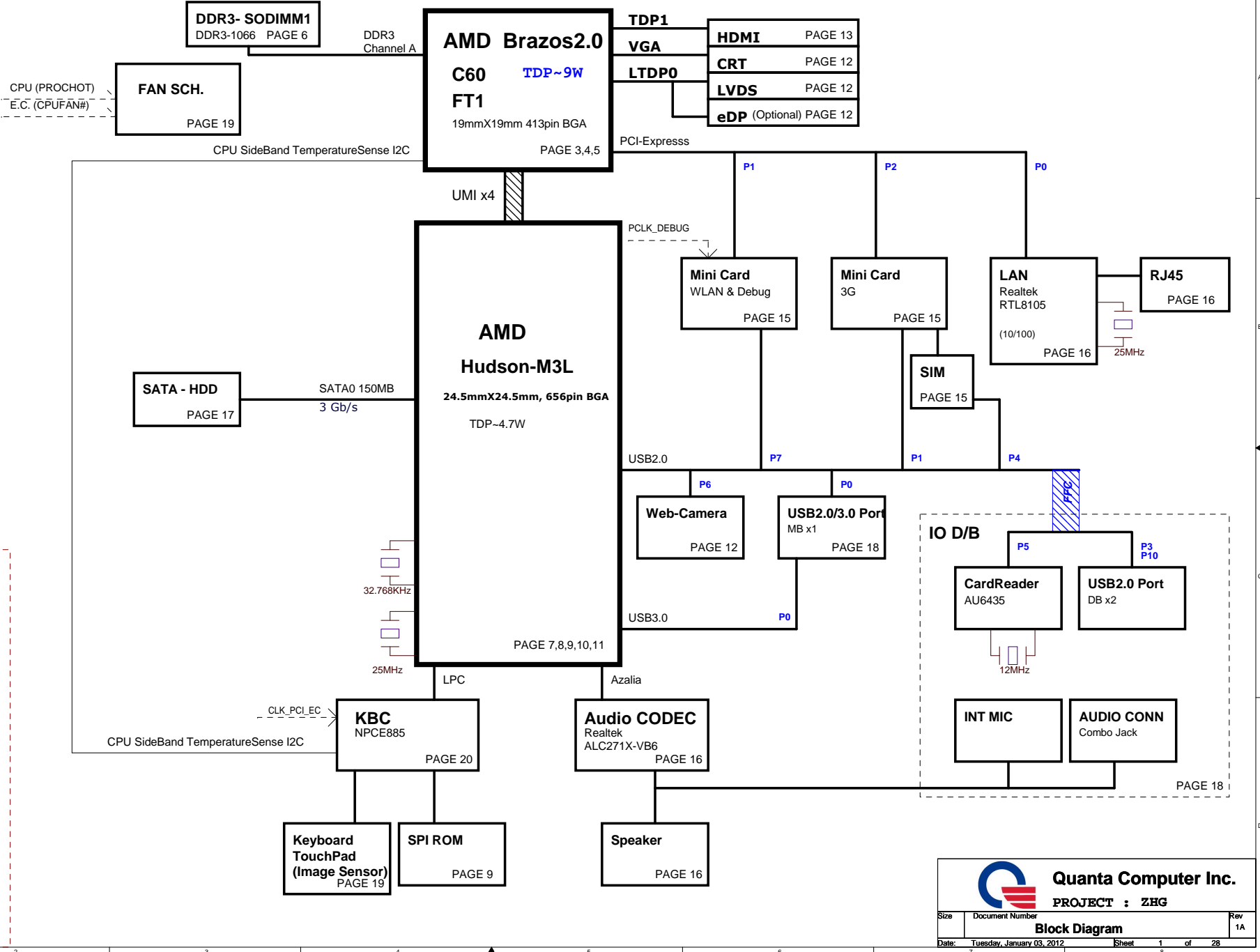
**1.05V (TPS51211)** PAGE 25 *NB*

**DDR 1.5V(TPS51216)** PAGE 26

**SYSTEM 5V/3V (RT8223P)** PAGE 22

**1.1V(TPS51211)** PAGE 24

**Discharge /Thermal protection** PAGE 27



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PROJECT : ZHG

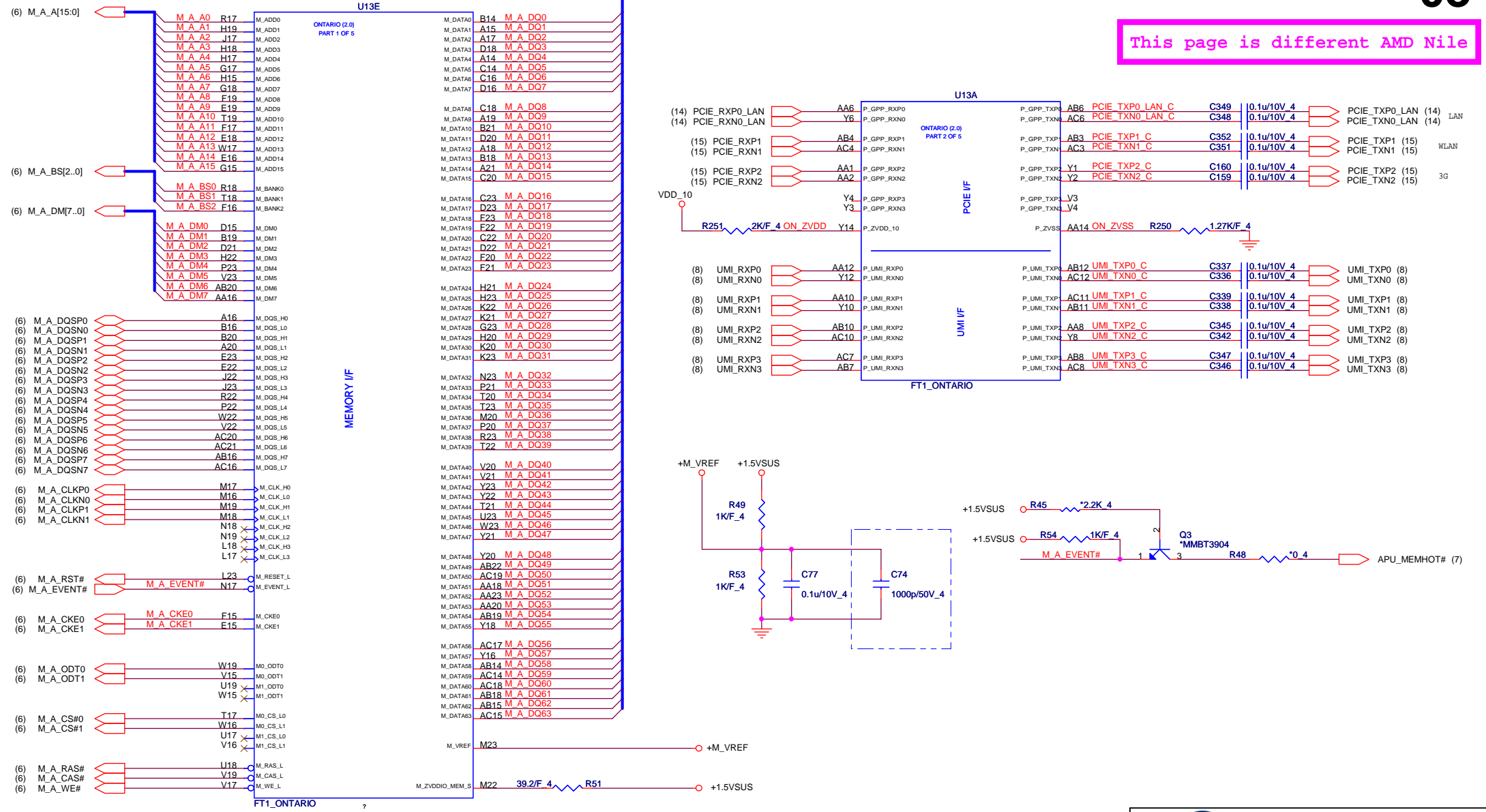
Size Document Number Rev 1A  
**Block Diagram**

Date: Tuesday, January 03, 2012 Sheet 1 of 28




(CPU)

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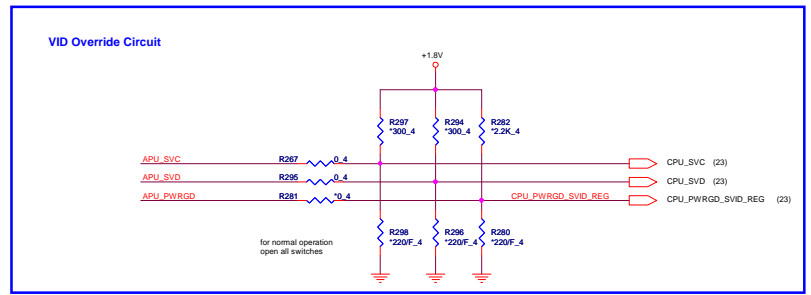
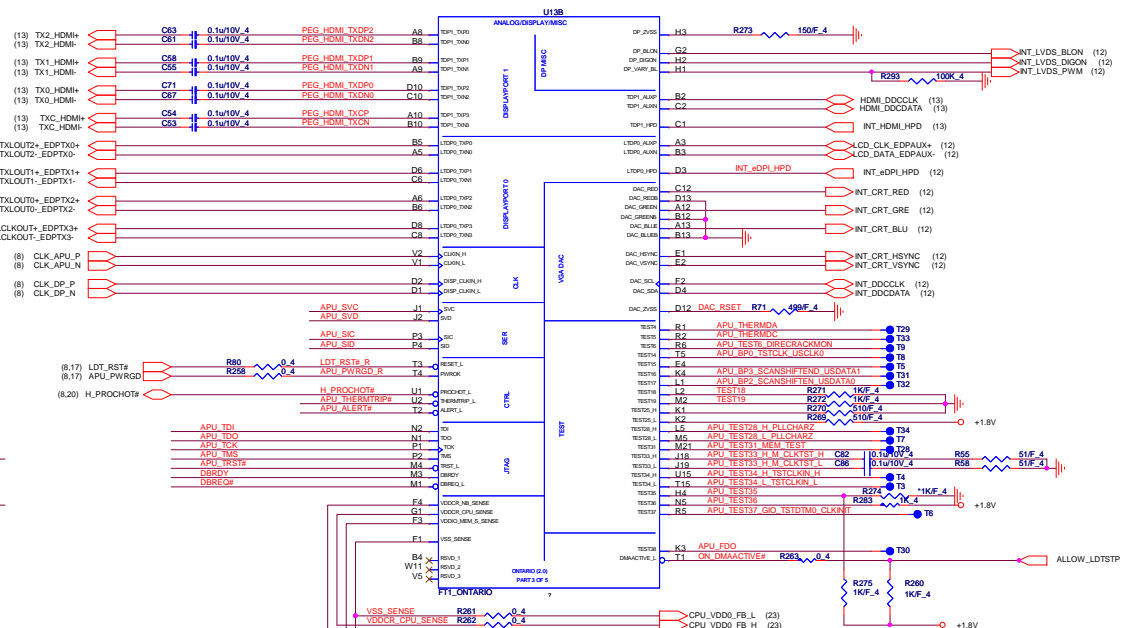
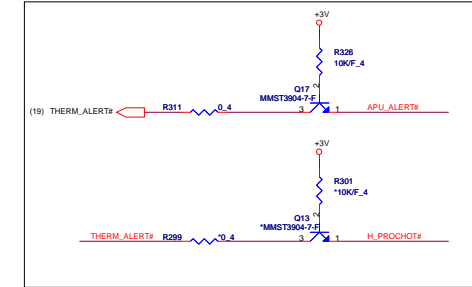
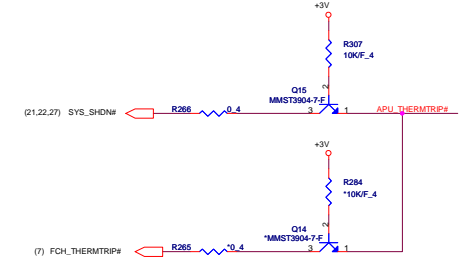
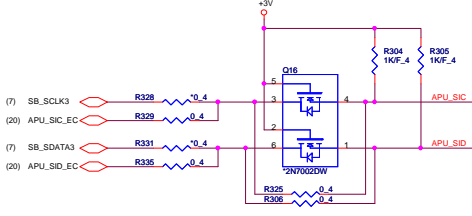
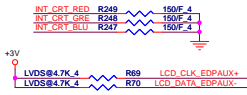
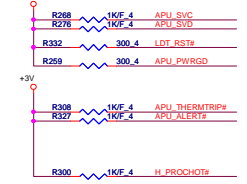
| P/N                                | Item Description |
|------------------------------------|------------------|
| AJ00C60VT00CPU (413P)CMC60AFPB22GV | 1.0G(BGA)        |
| AJ00C60VT01CPU (413P)CMC60AFPB22GV | 1.0G(BGA)STN BSQ |



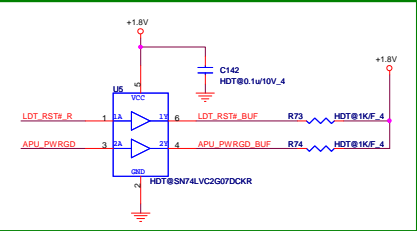
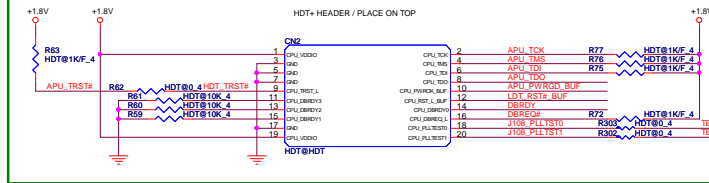
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PROJECT : ZHG

|       |  |               |
|-------|--|---------------|
| Size  | Document Number                        | Rev           |
|       | <b>ONTARIO MEM &amp; PCIE I/F(1/3)</b> | 1A            |
| Date: | Tuesday, January 10, 2012              | Sheet 3 of 28 |

(CPU)



HDT+ Connector(CPU)

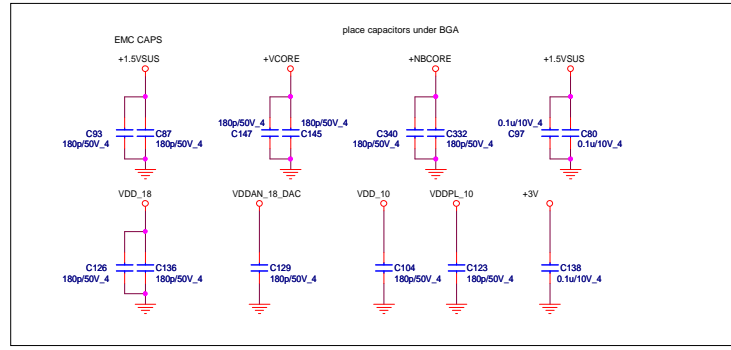
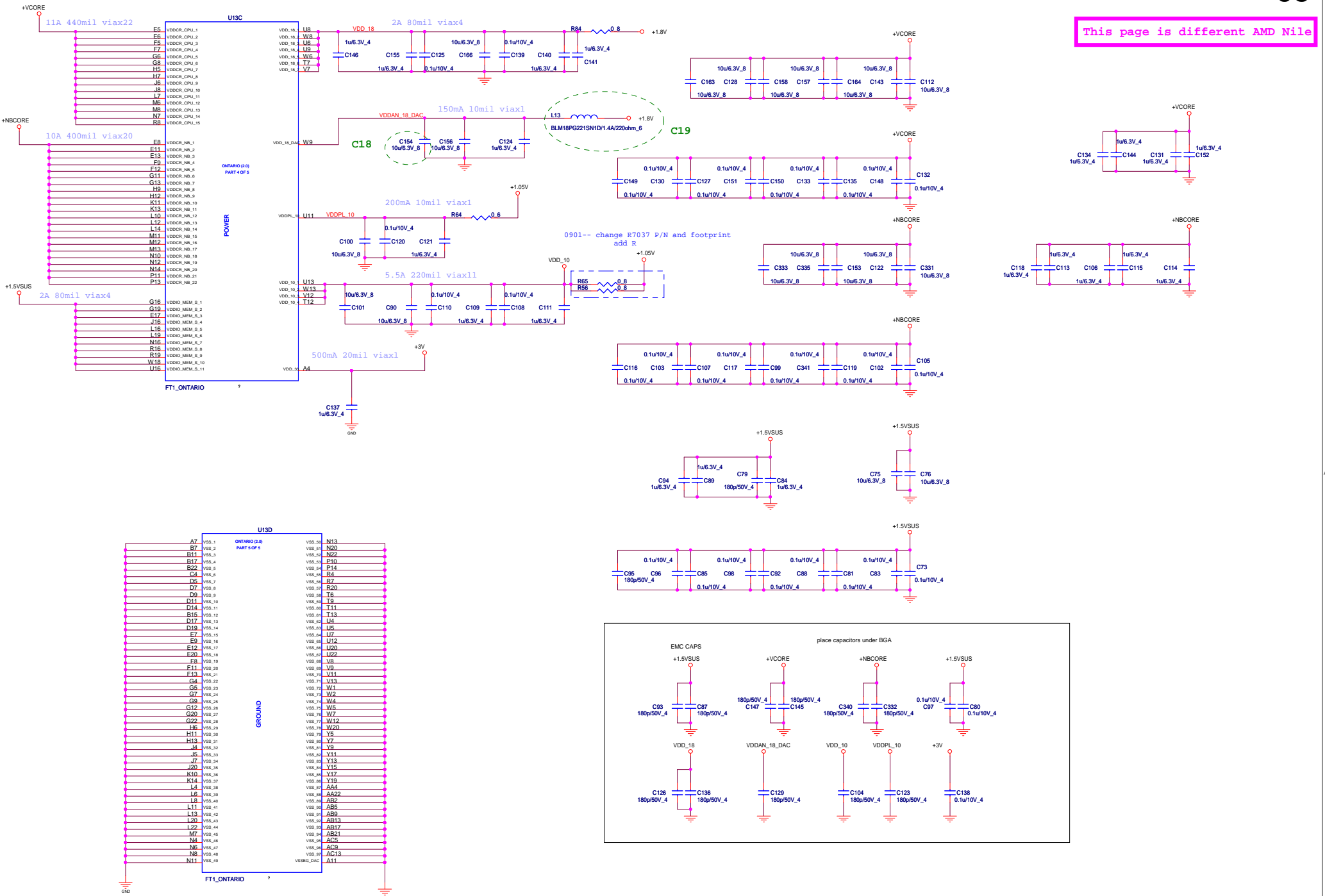


|            | 3     | 2   | 1   | 0   | DP AUX+   | DP AUX-  |
|------------|-------|-----|-----|-----|-----------|----------|
| HDMI       | Clock | CH0 | CH1 | CH2 | DDC Clock | DDC Data |
| LVDS Panel | Clock | CH0 | CH1 | CH2 | DDC Clock | DDC Data |
| eDP Panel  | ML3   | ML2 | ML1 | ML0 | AUX+      | AUX-     |

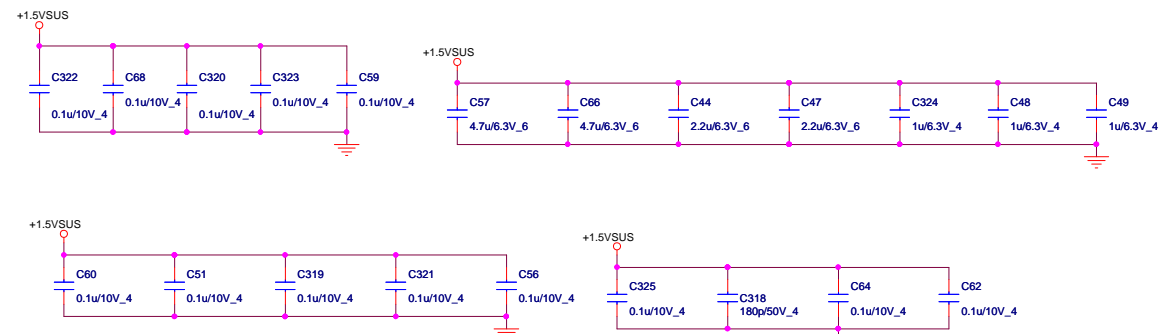
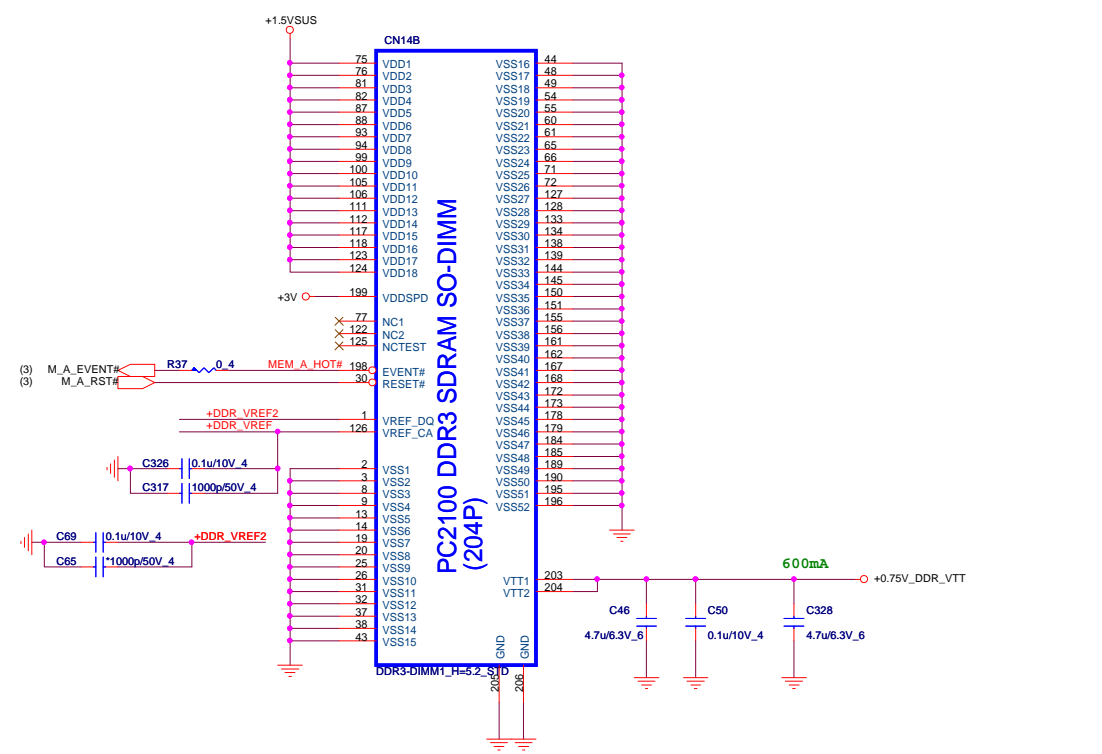
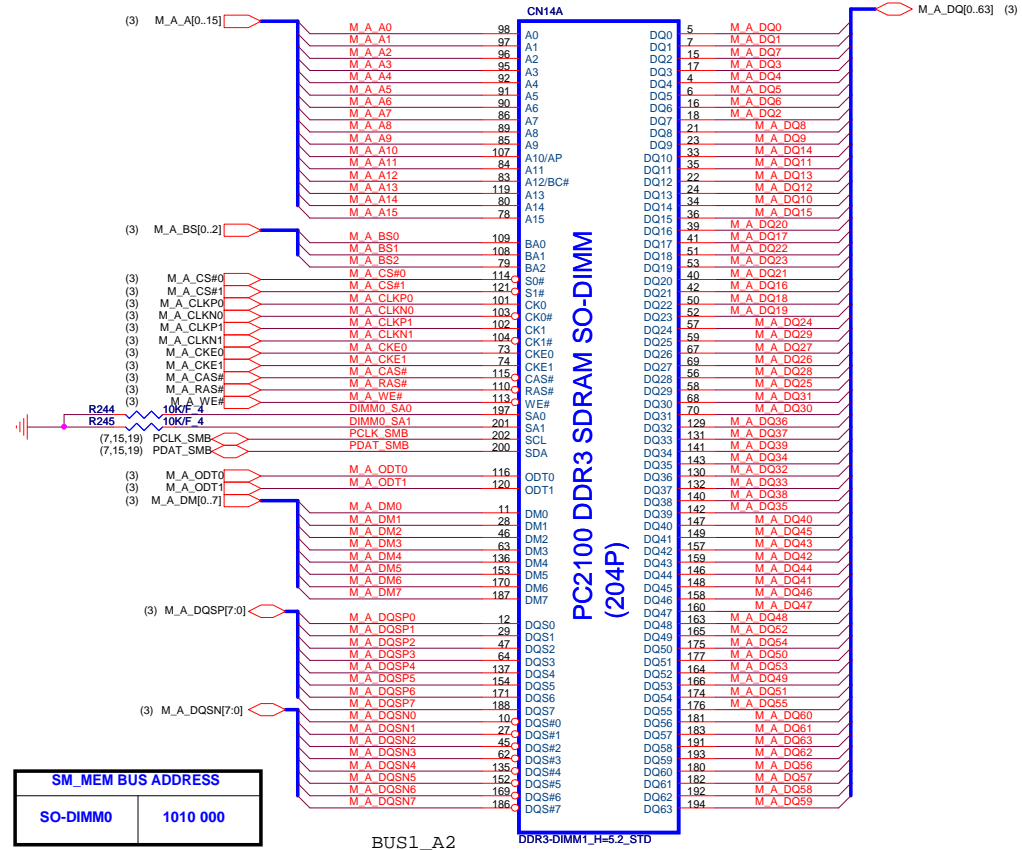
Eliminate the HDMI Output Disable Strapping Configuration TEST35 (ball H4) Remove "1k pull down" to VSS  
 Enable HDMI Output TEST35 (ball H4) Add 1K "pull up" to the VDD\_18 power rail

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(CPU)



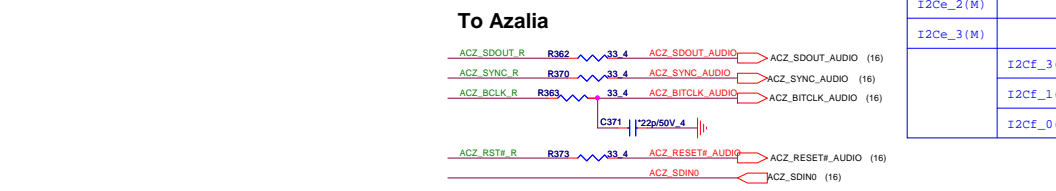
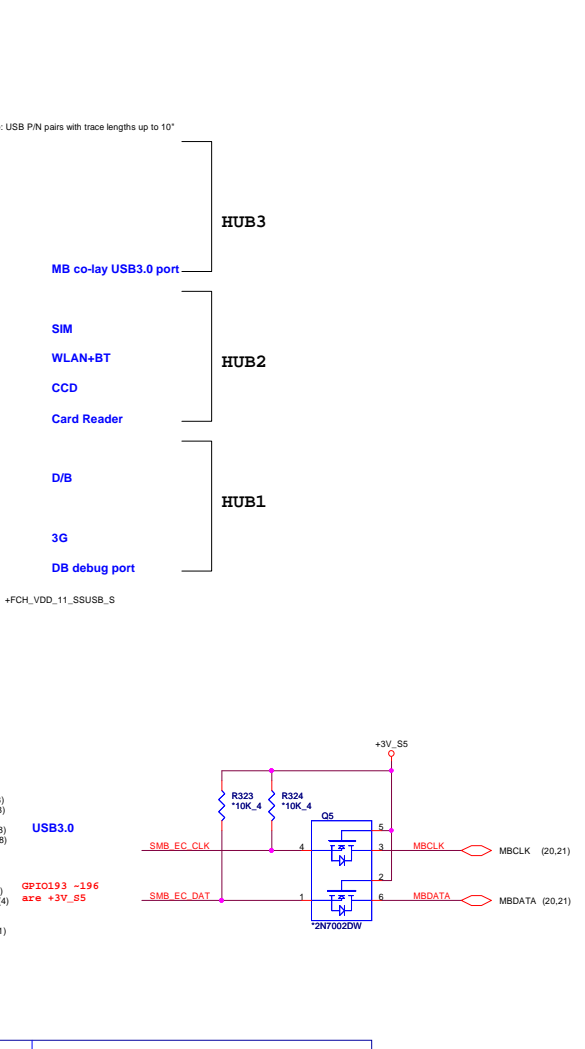
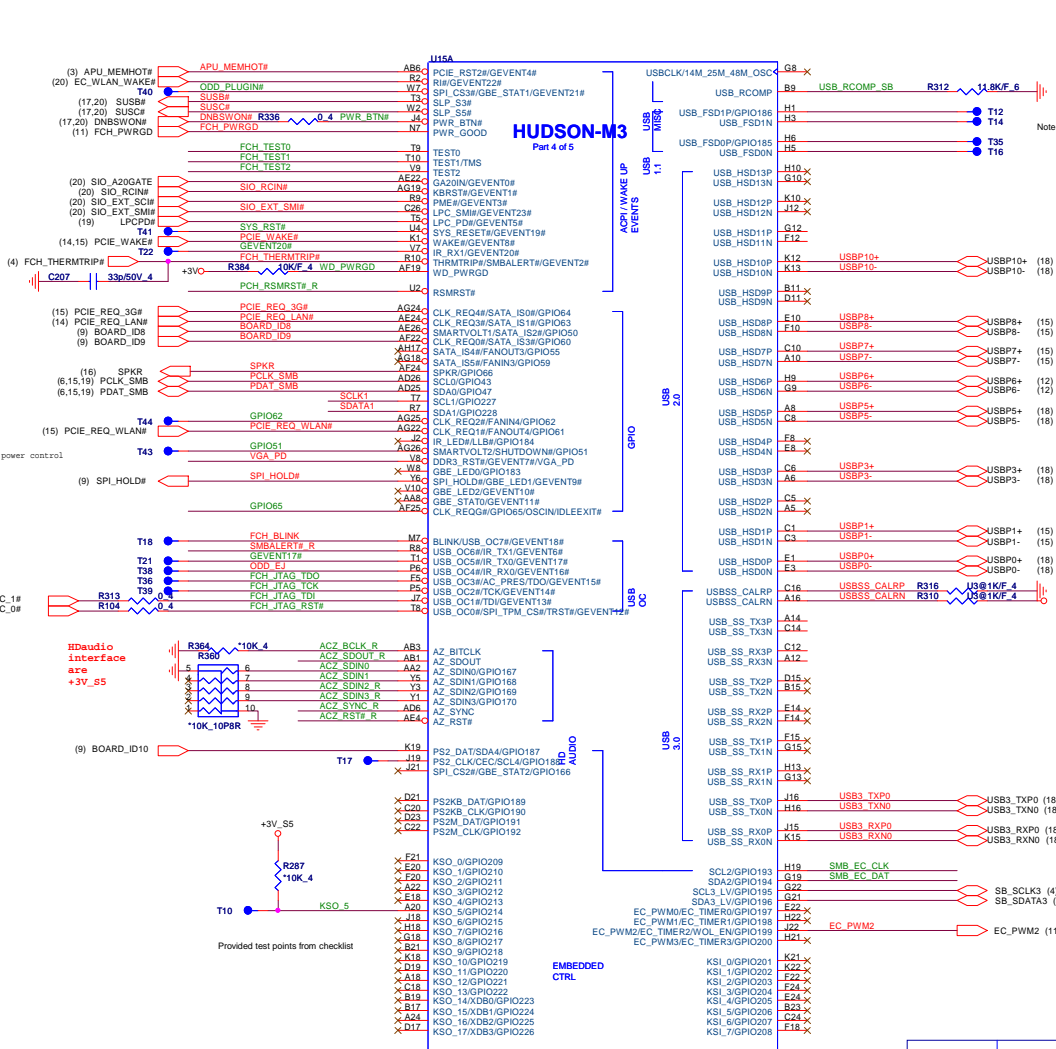
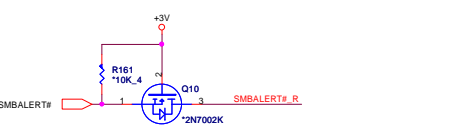
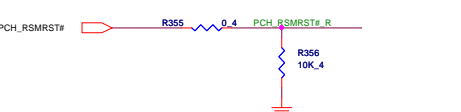
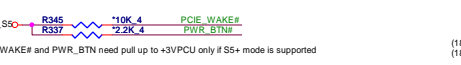
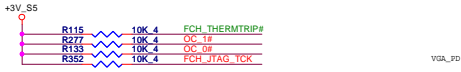
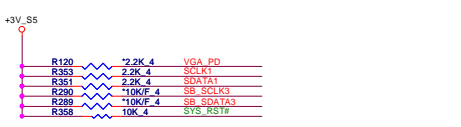
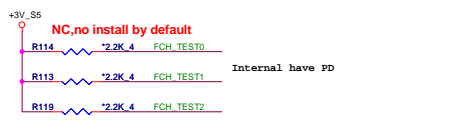
(DDR)



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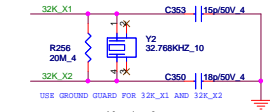
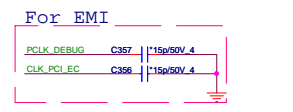
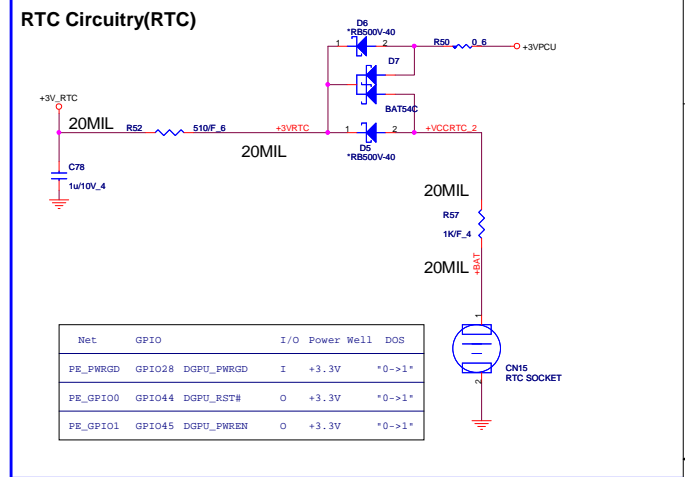
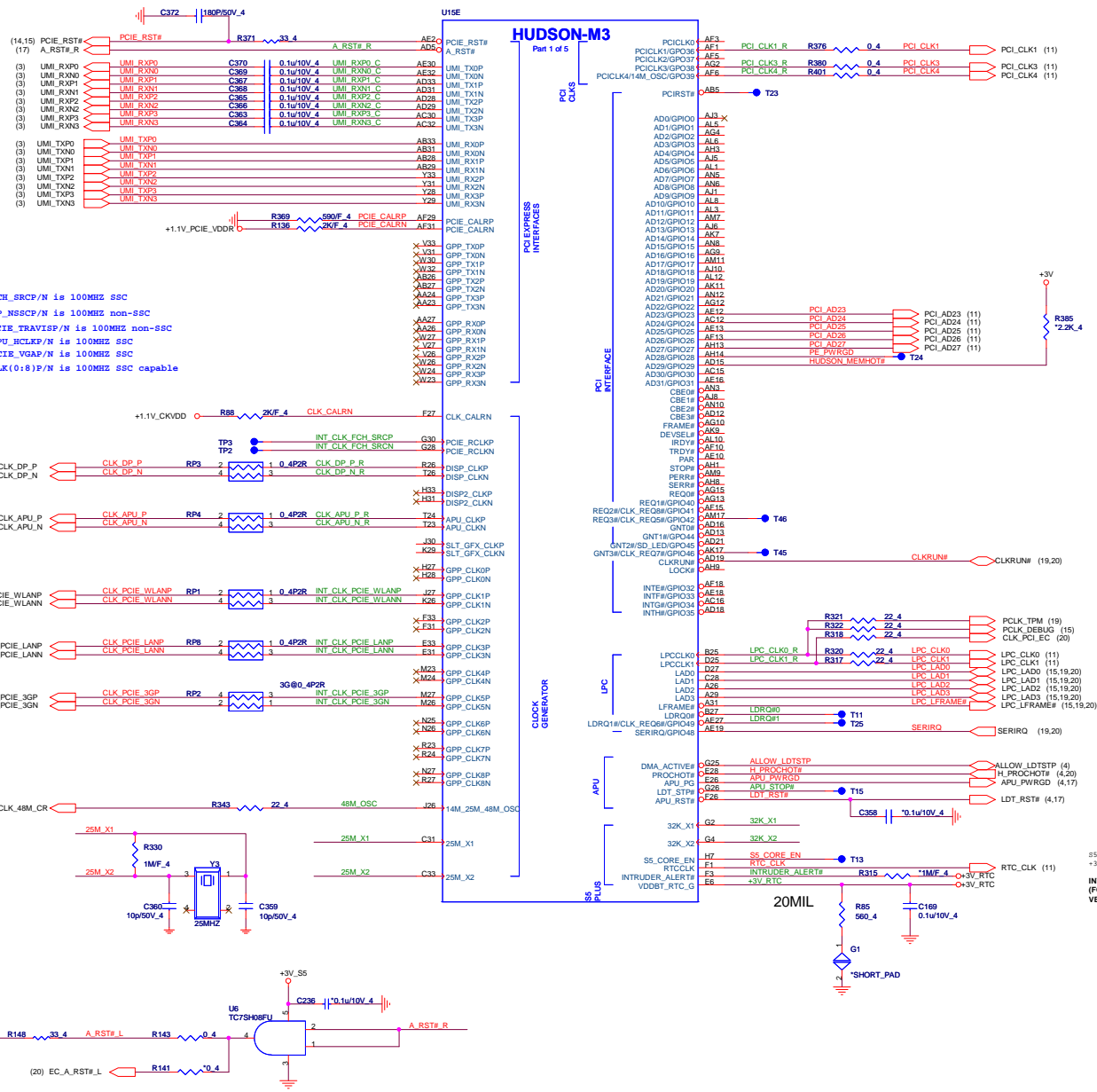
**PROJECT : ZHG**

|       |                           |               |
|-------|---------------------------|---------------|
| Size  | Document Number           | Rev           |
|       | <b>DDR3 SO-DIMM (STD)</b> | 1A            |
| Date: | Tuesday, January 10, 2012 | Sheet 6 of 28 |



| EC        | FCH       | Device  | I2C_Device(S) |
|-----------|-----------|---------|---------------|
| I2Ce_1(M) | I2Cf_2(M) | Charger | Battery       |
| I2Ce_2(M) |           | APU     |               |
| I2Ce_3(M) |           | APU     |               |
|           | I2Cf_3(M) |         |               |
|           | I2Cf_1(M) |         |               |
|           | I2Cf_0(M) | DDR     | WLAN/3G       |
|           |           |         | Image Sensor  |
|           |           |         | S0            |

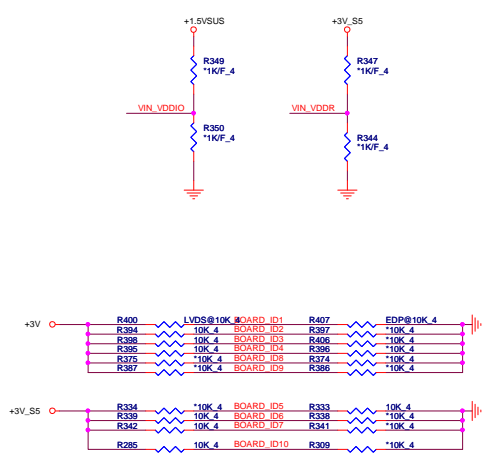
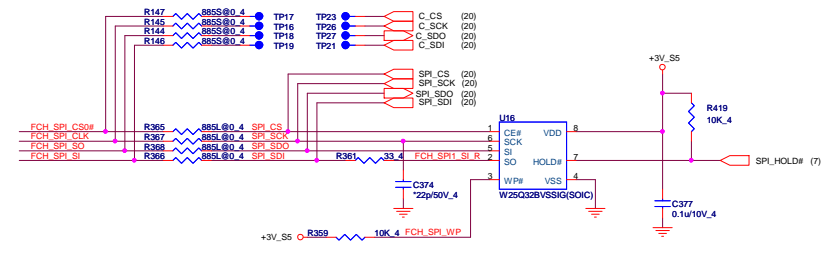
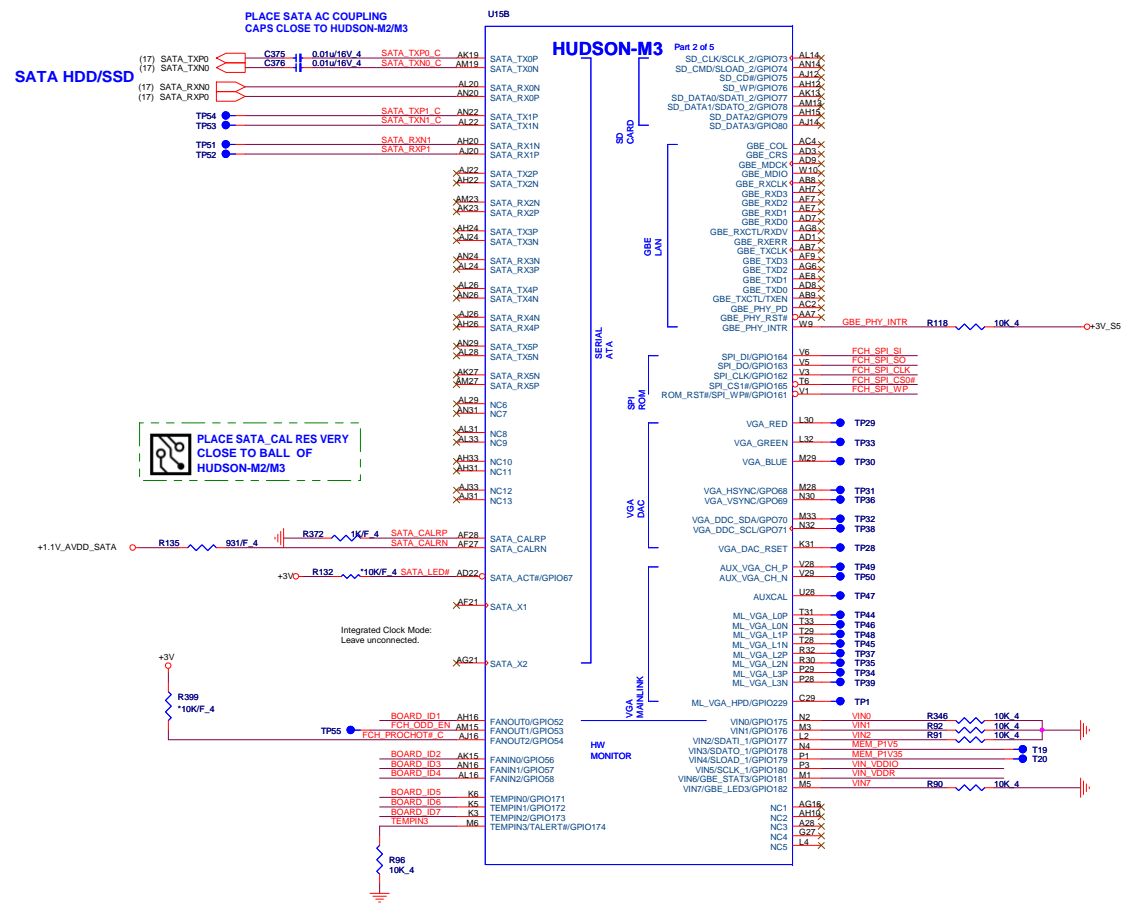
EC will Conflict with FCH. Do not mount



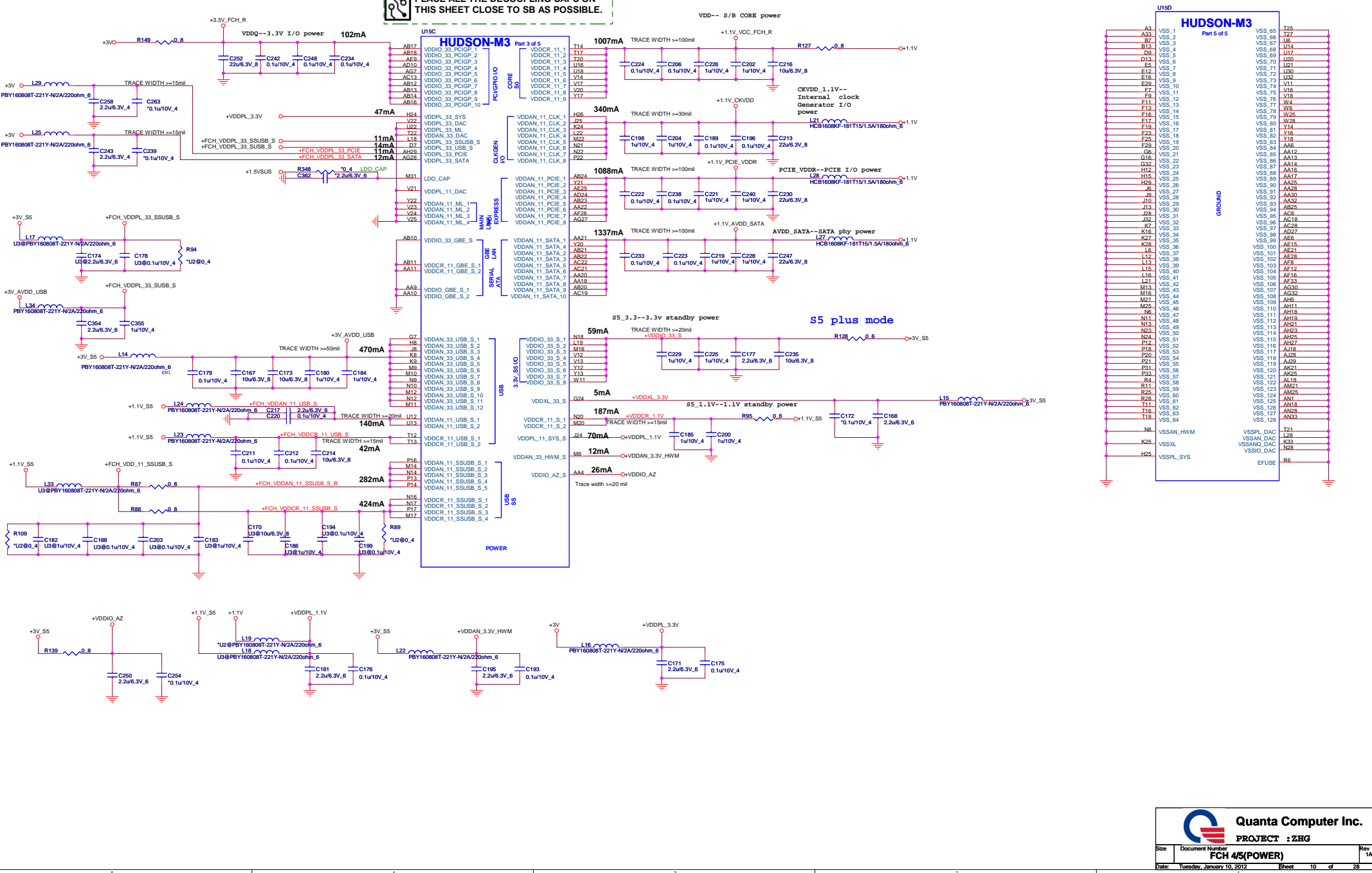
SS\_CORE\_EN is necessary to connect enable pin of +3VDC/+5VDCU regulator for S+ mode implementation

INTRUDER\_ALERT# Left not connected (FCH has 50-kohm internal pull-up to VBAT.)



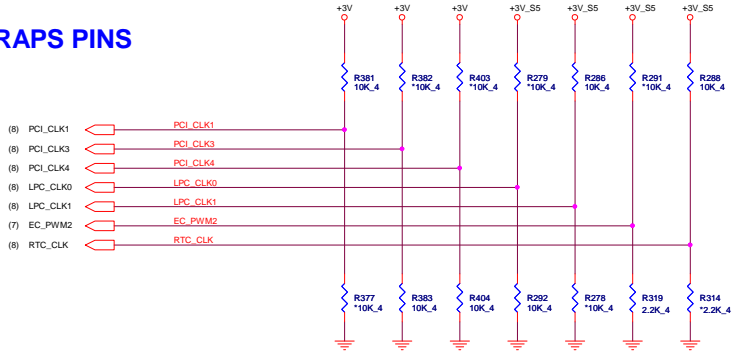


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



**OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.**

**STRAPS PINS**



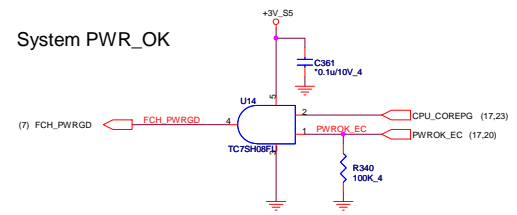
EC\_PWM2 ->  
SPI ROM: 2.2-KΩ 5t pull-down  
LPC ROM: Pull-up to 3.3V\_S5.  
External pull-up resistor is not required as FCH is integrated 10-KΩ pull-up to 3.3V\_S5.

Remove PCI\_CLK2 function

**REQUIRED STRAPS**

|                  | ----- | PCI_CLK1                   | PCI_CLK2 | PCI_CLK3                      | PCI_CLK4                     | LPC_CLK0               | LPC_CLK1                  | EC_PWM2            | RTC_CLK                             |
|------------------|-------|----------------------------|----------|-------------------------------|------------------------------|------------------------|---------------------------|--------------------|-------------------------------------|
| <b>PULL HIGH</b> | ----- | ALLOW PCIE Gen2<br>DEFAULT | -----    | USE DEBUG STRAP               | non_Fusion CLOCK MODE        | EC ENABLED             | CLKGEN ENABLED<br>DEFAULT | LPC ROM            | S5 PLUS MODE<br>DISABLED<br>DEFAULT |
| <b>PULL LOW</b>  | ----- | FORCE PCIE Gen1            | -----    | IGNORE DEBUG STRAP<br>DEFAULT | FUSION CLOCK MODE<br>DEFAULT | EC DISABLED<br>DEFAULT | CLKGEN DISABLED           | SPI ROM<br>DEFAULT | S5 PLUS MODE<br>ENABLED             |

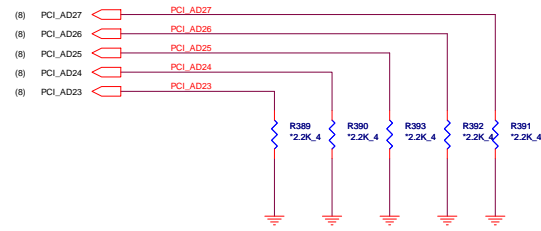
**System PWR\_OK**



**FCH\_PWRGD CKT**

**DEBUG STRAPS**

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

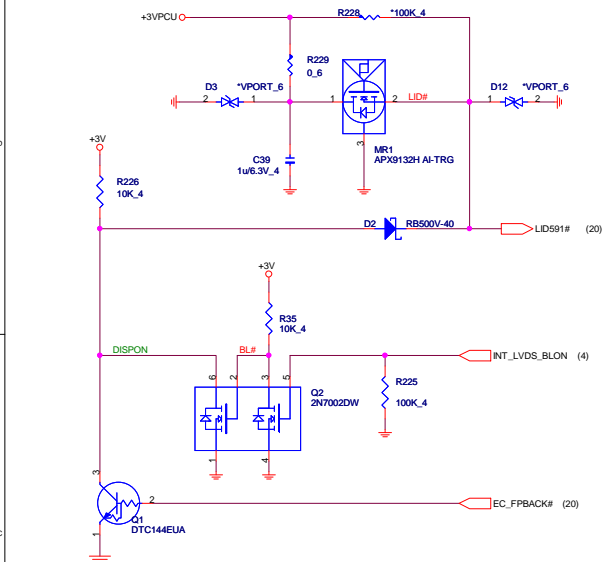


|                  | PCI_AD27               | PCI_AD26                       | PCI_AD25              | PCI_AD24                           | PCI_AD23                        |
|------------------|------------------------|--------------------------------|-----------------------|------------------------------------|---------------------------------|
| <b>PULL HIGH</b> | USE PCI PLL<br>DEFAULT | DISABLE ILA AUTORUN<br>DEFAULT | USE FC PLL<br>DEFAULT | USE DEFAULT PCIE STRAPS<br>DEFAULT | DISABLE PCI MEM BOOT<br>DEFAULT |
| <b>PULL LOW</b>  | BYPASS PCI PLL         | ENABLE ILA AUTORUN             | BYPASS FC PLL         | USE EEPROM PCIE STRAPS             | ENABLE PCI MEM BOOT             |

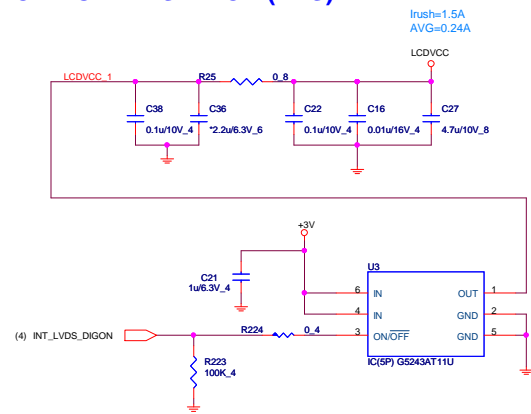
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PROJECT : ZHG

Size: Document Number: FCH 5/5(STRAP & PWRGD) Rev: 1A  
Date: Tuesday, January 10, 2012 Sheet: 11 of 28

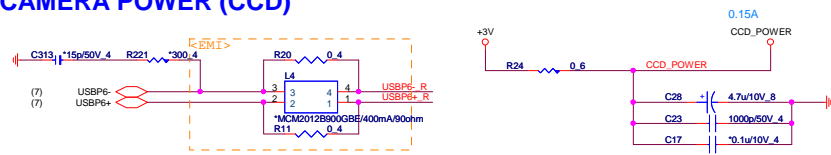
## HALL IC (HSR)



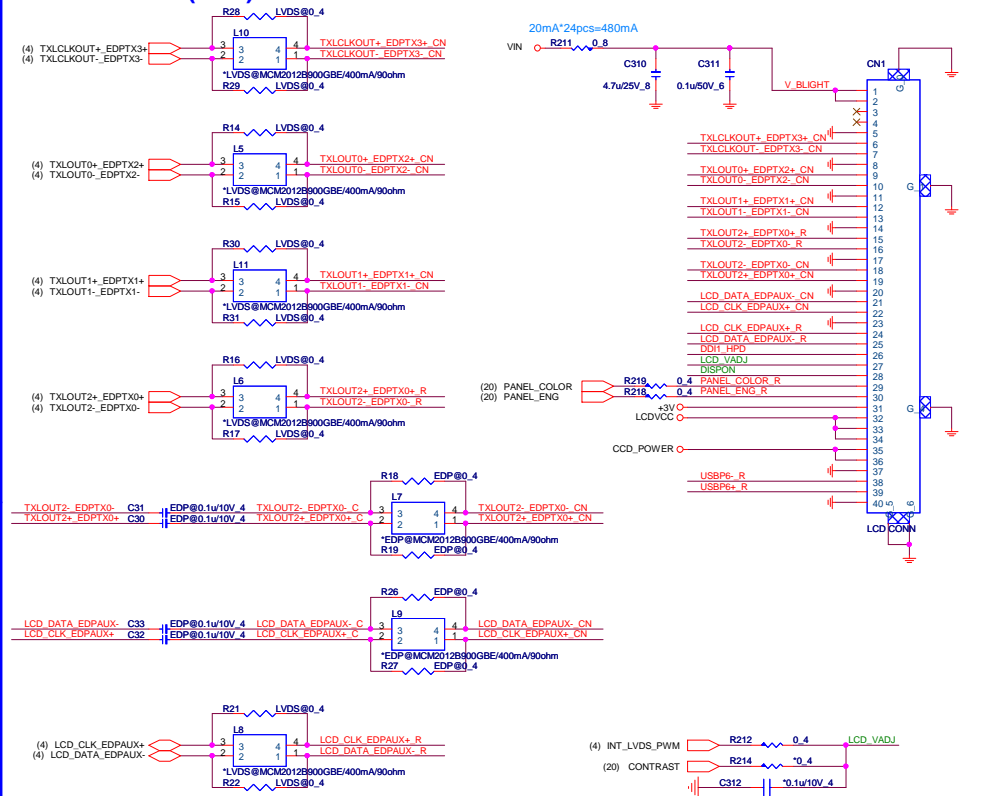
## LCD POWER SWITCH (LDS)



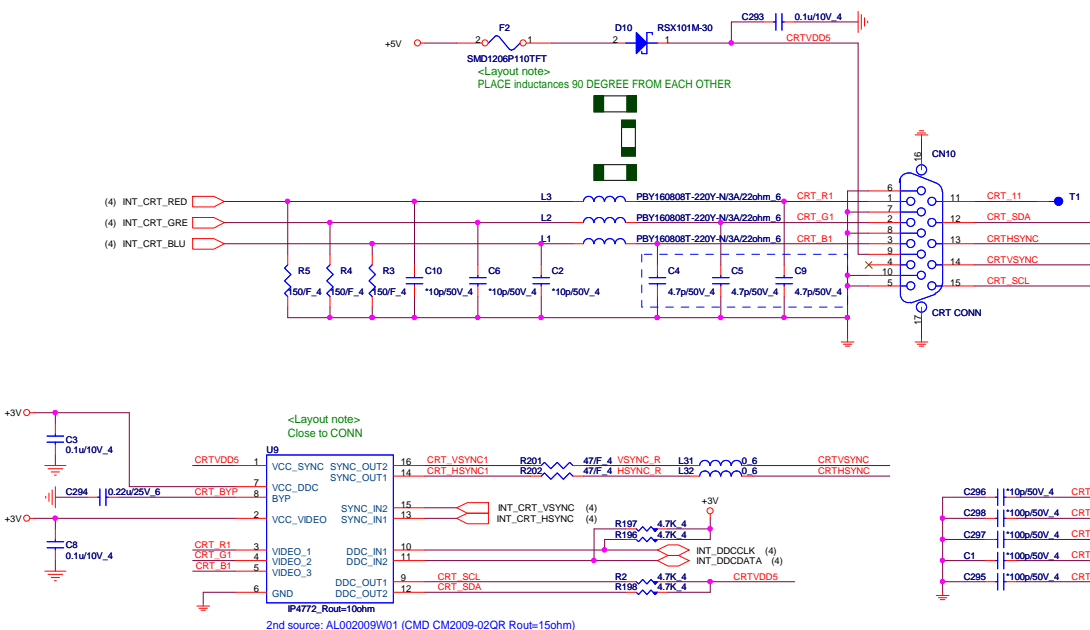
## CAMERA POWER (CCD)



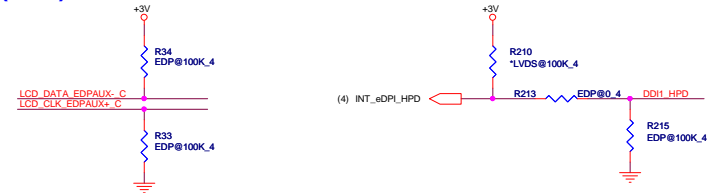
## LCD MODULE (LDS)



## CRT(CRT)

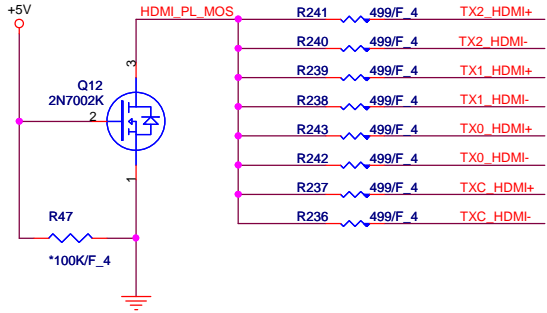


## eDP (LDS)

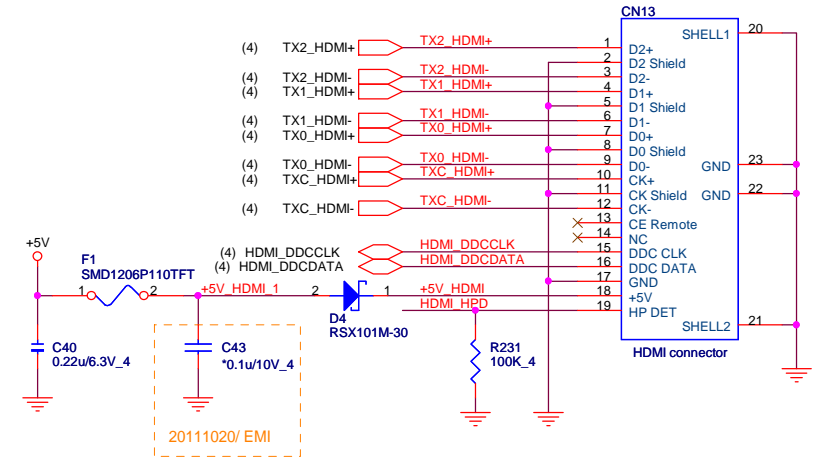
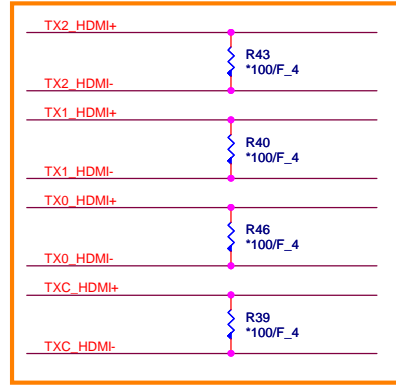


# HDMI (HDM)

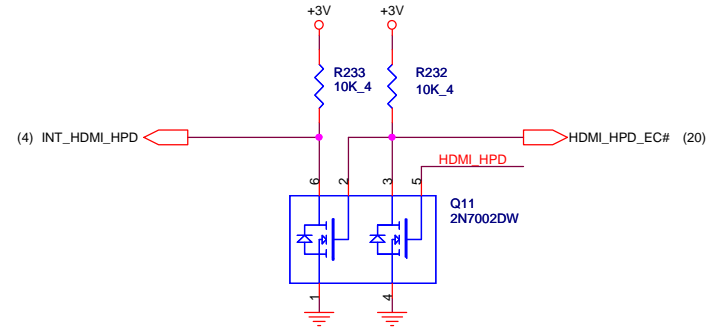
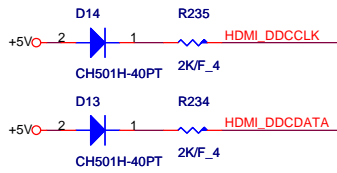
## Close to HDMI Connector



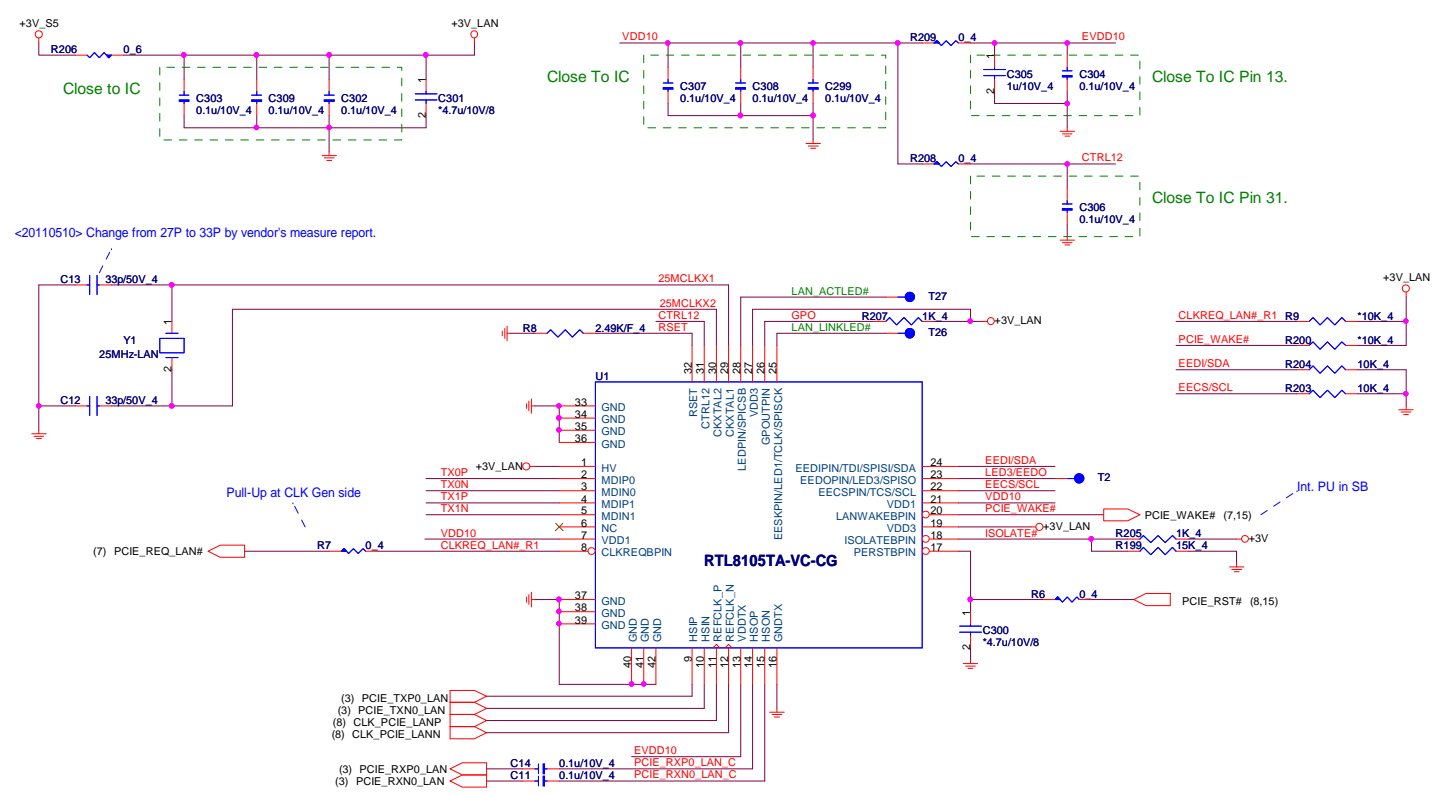
## EMI reserve for HDMI



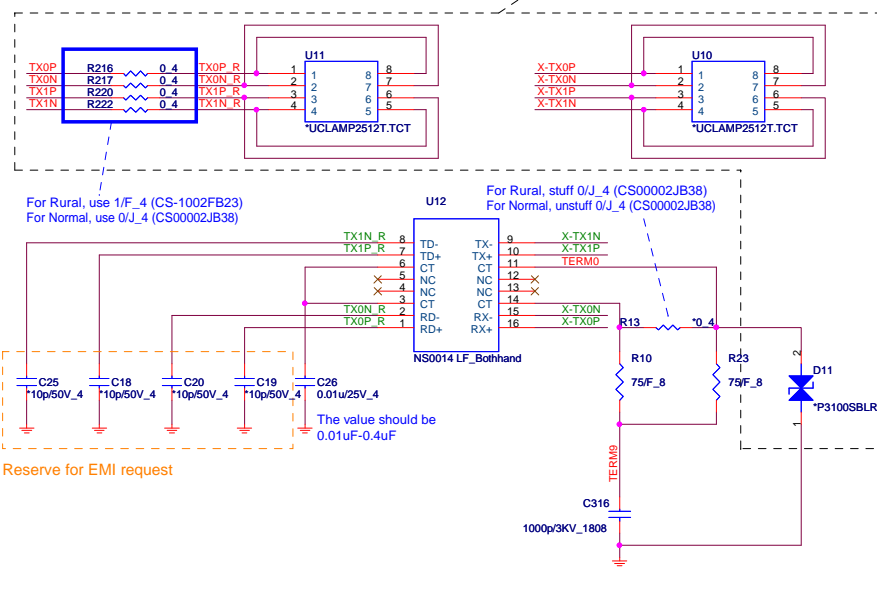
## SDVO I2C Control (HDM)



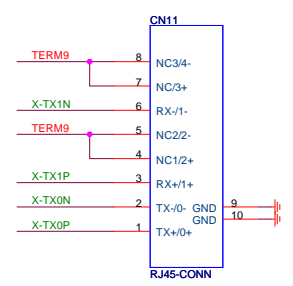
## LAN (LAN)




## TRANSFORMER (LAN)



## RJ45 Connector (LAN)

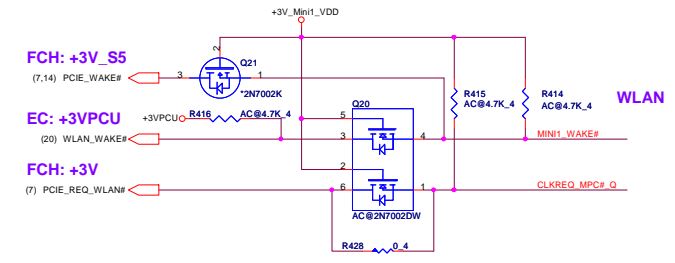
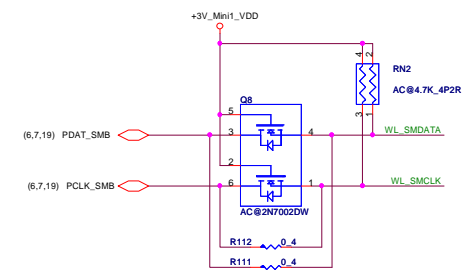
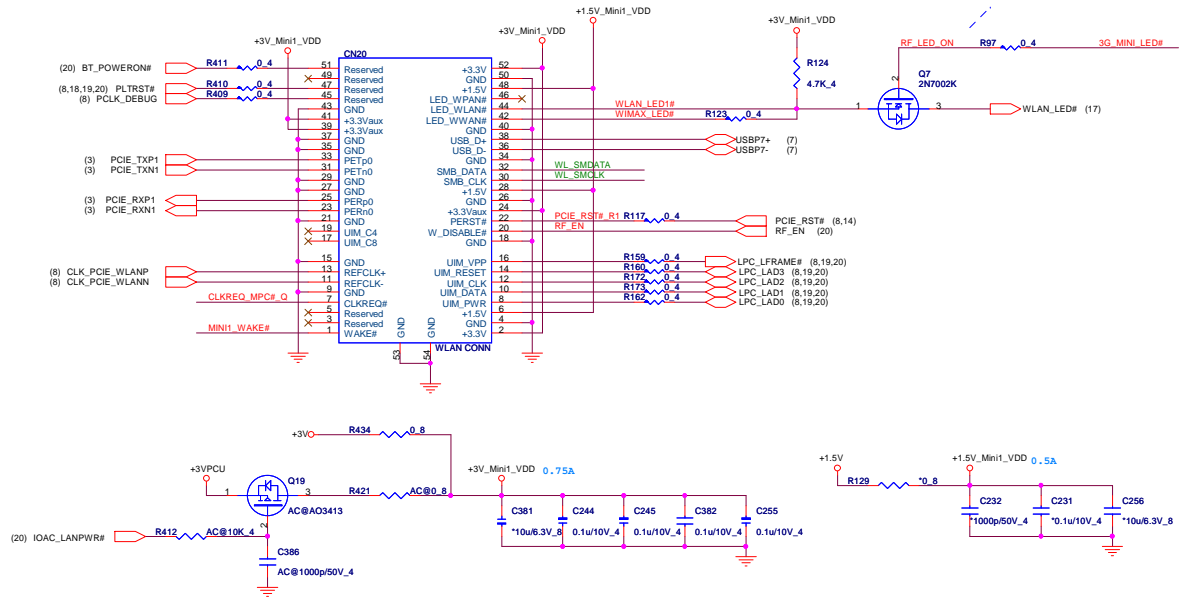




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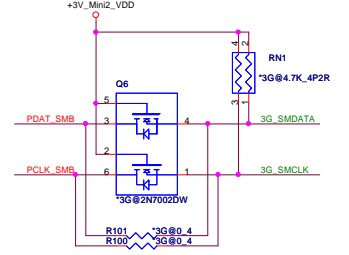
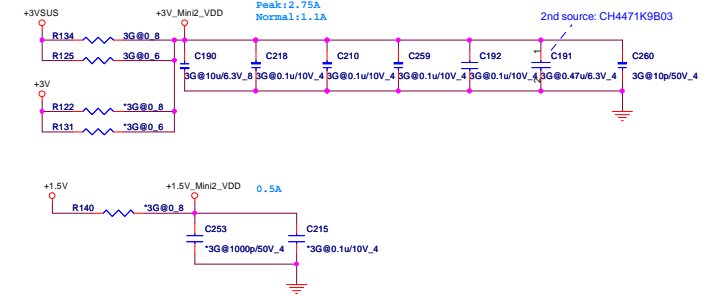
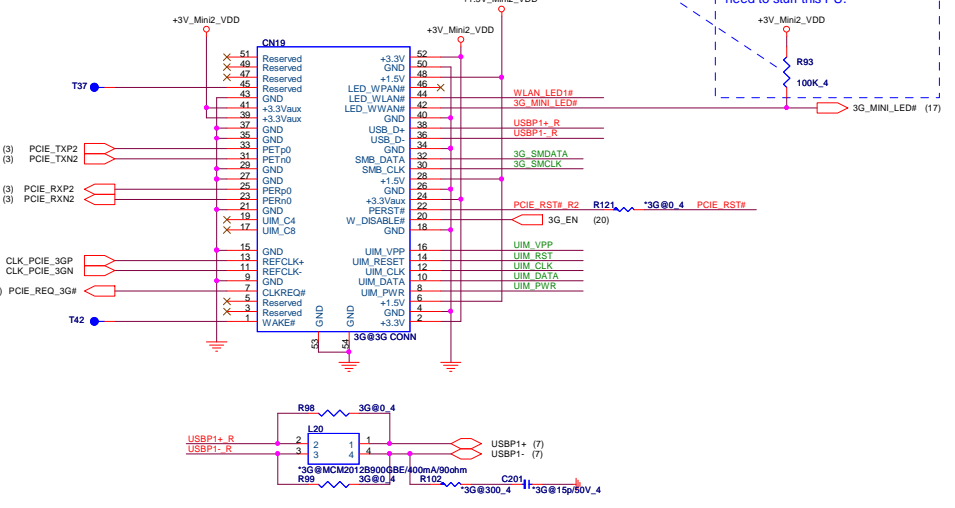
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|-------|----------------------------|-------|----------|
| Size  | Document Number            | Rev   |          |
|       | <b>LAN RTL8105TA-VC-CG</b> | 1A    |          |
| Date: | Tuesday, January 10, 2012  | Sheet | 14 of 28 |

# Mini Card 1 (MPC)



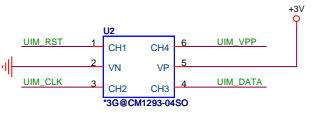
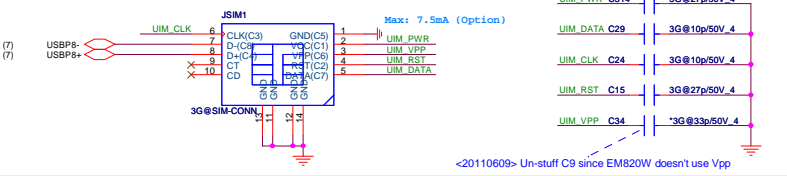
# Mini Card 2 (MNC)

<2011/24(E1A)> Change from 10k to 100k to reduce leakage  
 no matter have 3G function or not, need to stuff this PU.

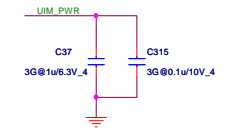


# MultiMedia SIM (MNC)

<Layout Notes> Keep USIM signals max length within 8000mils.

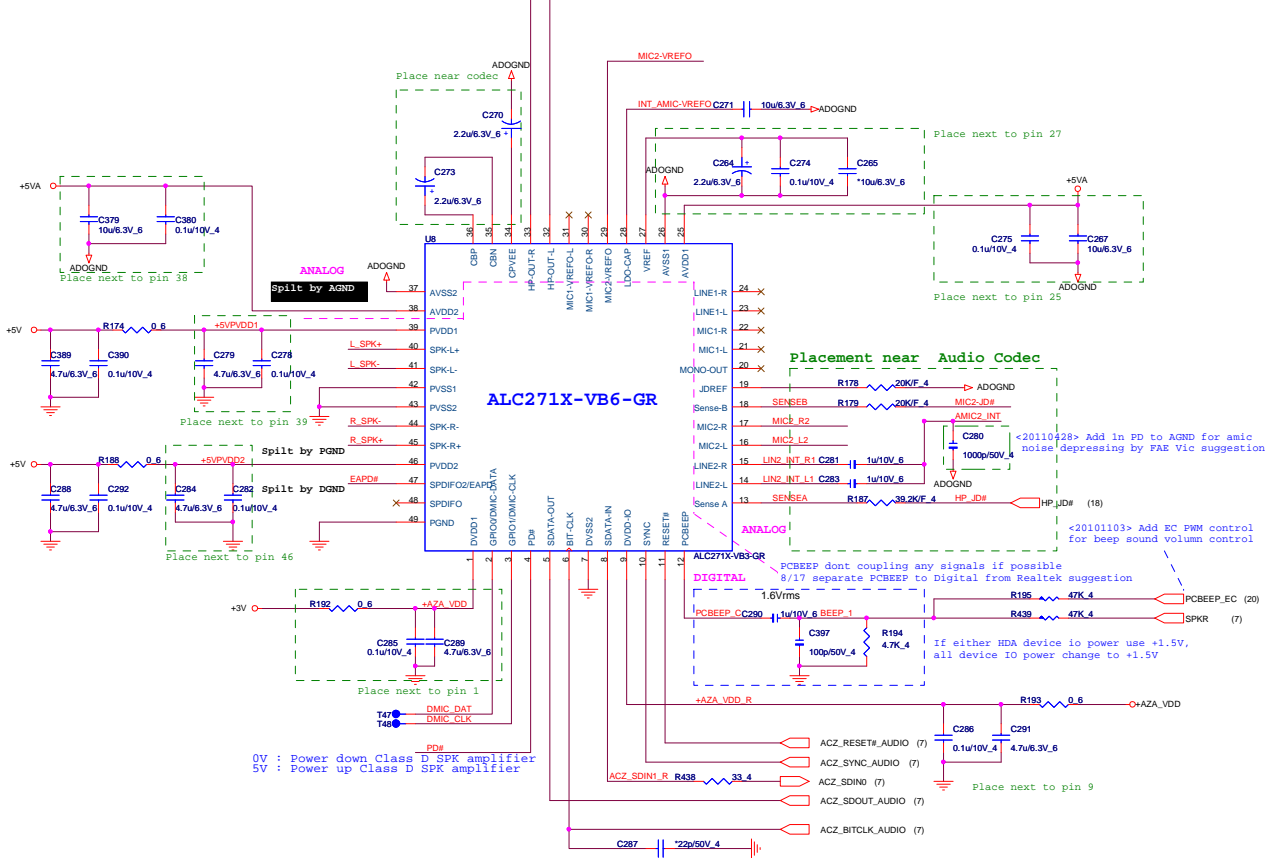


<20090604(A1A)\_Qualcomm design guide>  
 Place 0.1uF near connector's VCC pin

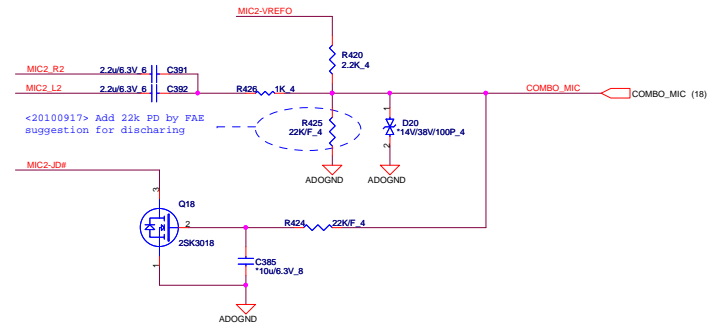


<20110609> Un-stuff C9 since EM820W doesn't use Vpp

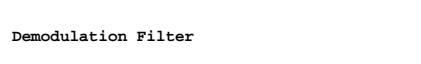
# Codec ALC271X (ADO)



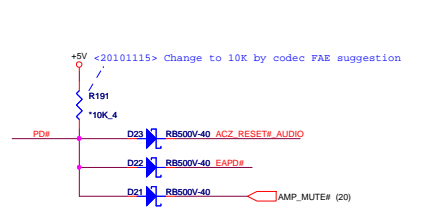
# EARPHONE (AMP)



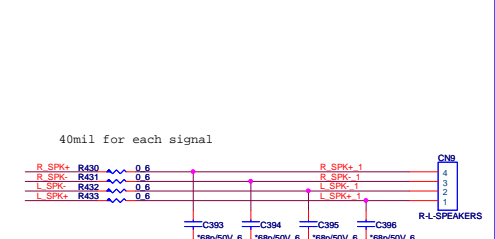
# Power (ADO)



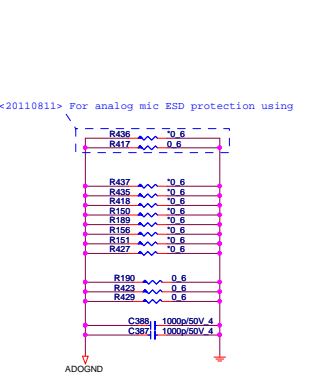
# Mute (ADO)



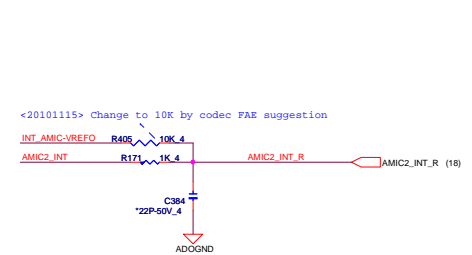
# Internal Speaker (AMP)



# GND(ADO)

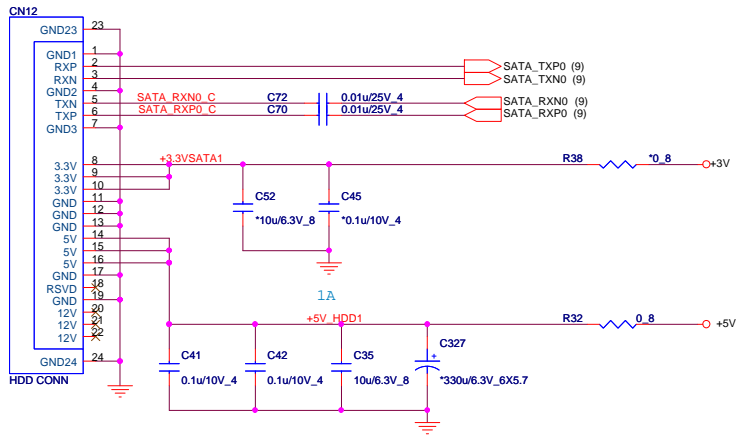


# Internal Analog MIC (AMP)

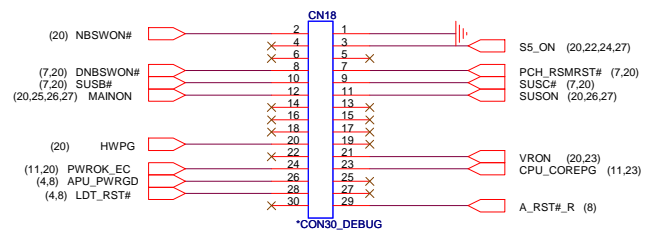




# 2.5" SATA HDD (HDD)

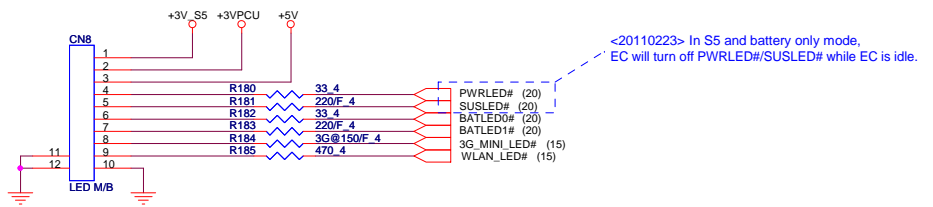


# Power Sequence Connector(CPU)

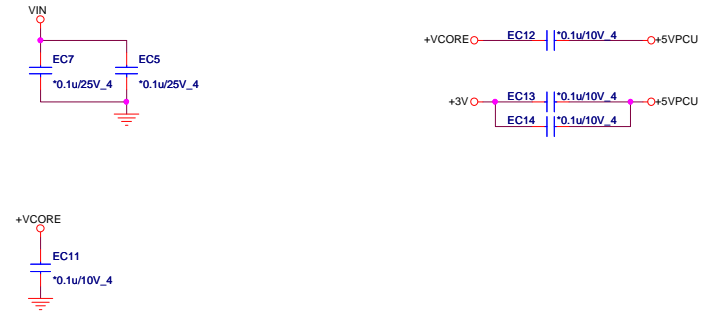


|    |             |    |         |    |            |
|----|-------------|----|---------|----|------------|
| 1  | GND         | 11 | SUSON   | 21 | VRON       |
| 2  | NBSWON#     | 12 | MAINON  | 22 | RESERVE    |
| 3  | S5_ON       | 13 | RESERVE | 23 | CPU_COREPG |
| 4  | RESERVE     | 14 | RESERVE | 24 | PWROK_EC   |
| 5  | RESERVE     | 15 | RESERVE | 25 | RESERVE    |
| 6  | RESERVE     | 16 | RESERVE | 26 | APU_PWRGD  |
| 7  | PCH_RSMRST# | 17 | RESERVE | 27 | RESERVE    |
| 8  | DNBSWON#    | 18 | RESERVE | 28 | LDT_RST#   |
| 9  | SUSC#       | 19 | RESERVE | 29 | A_RST#_R   |
| 10 | SUSB#       | 20 | HWPG    | 30 | RESERVE    |

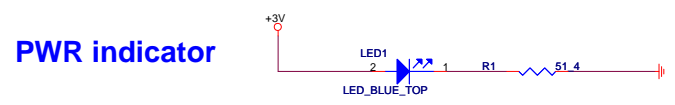
# LED DB (UIF)




# Stitching Cap(EMC)



# POWER LED(UIF)

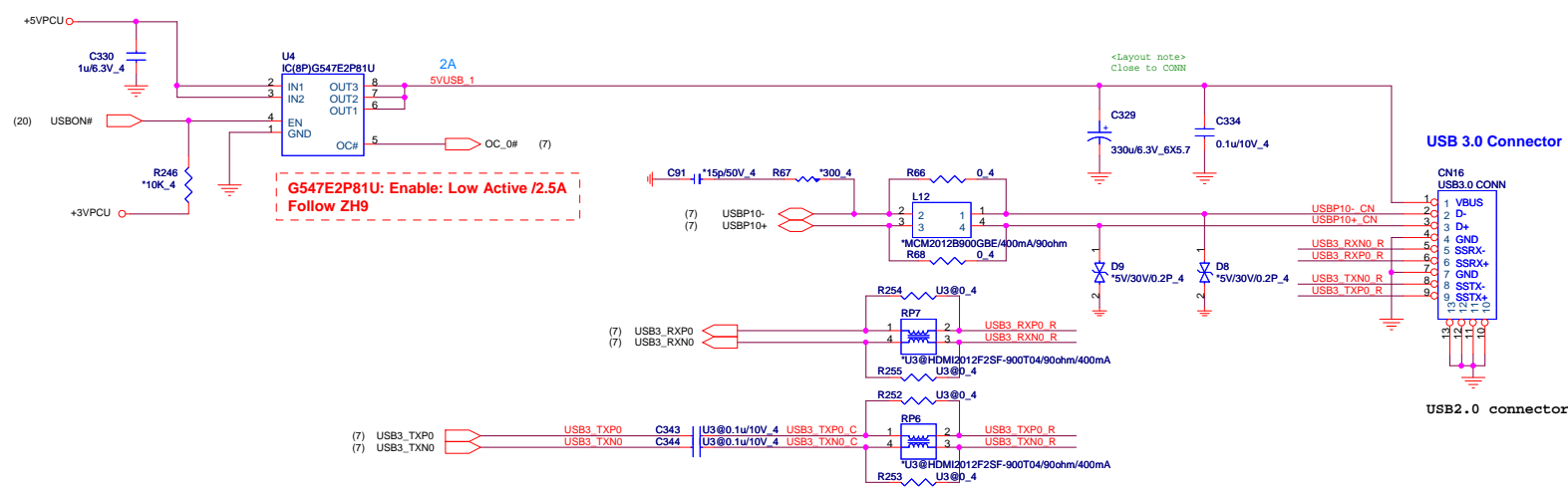




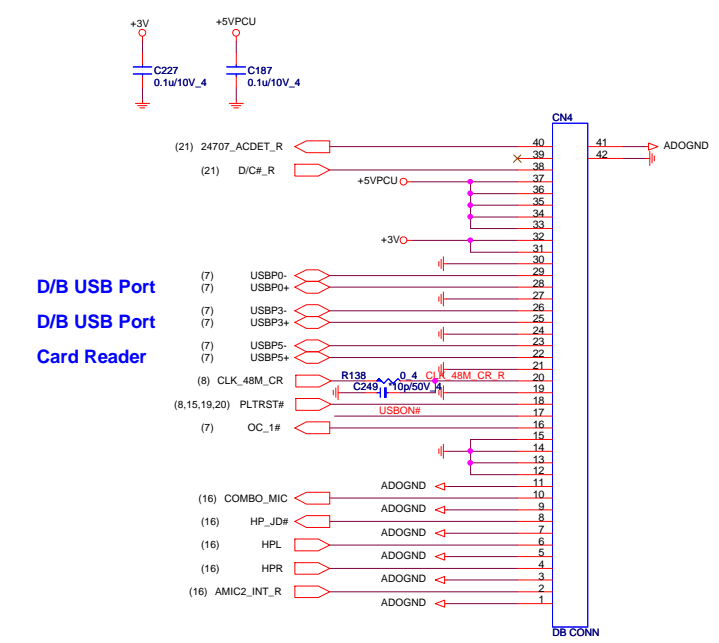
**Quanta Computer Inc.**  
PROJECT : ZHG

|       |                           |                |
|-------|---------------------------|----------------|
| Size  | Document Number           | Rev            |
|       | <b>SATA HDD/LED/SW</b>    | 1A             |
| Date: | Tuesday, January 10, 2012 | Sheet 17 of 28 |

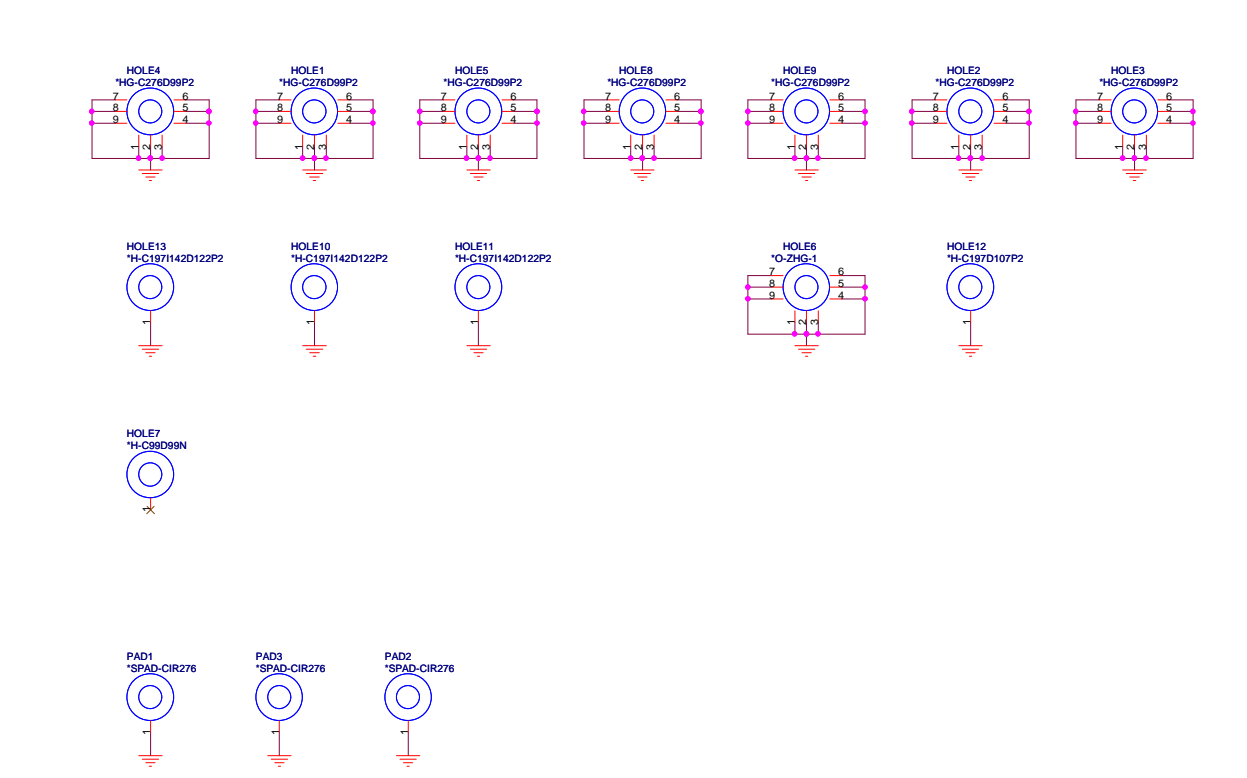
# USB Left (USB)



# IO D/B (UIF)



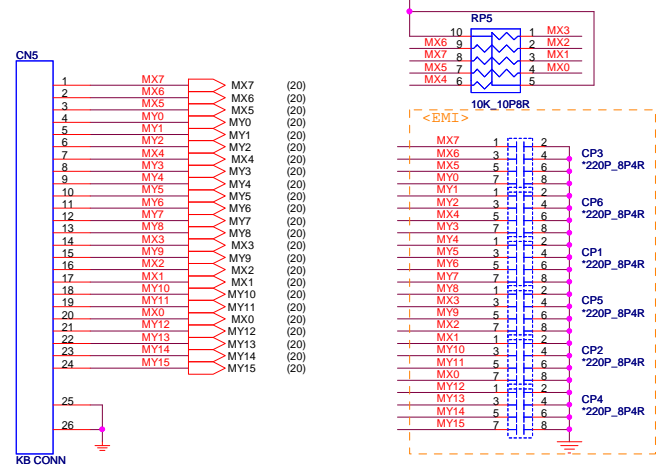
# HOLE(OTH)



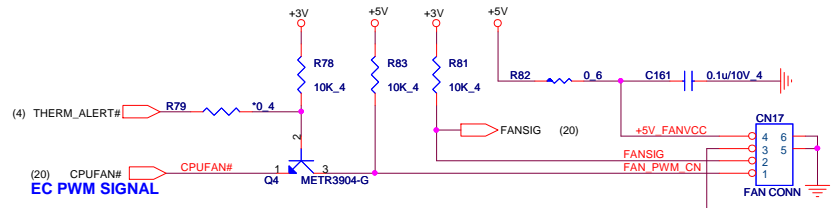
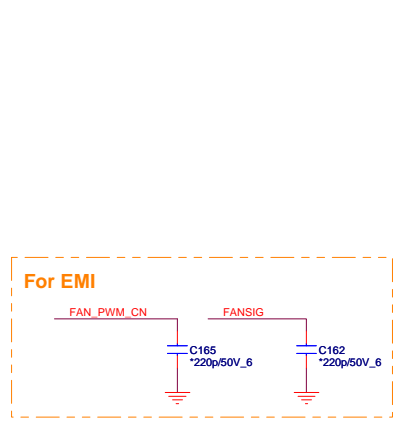
# POWER M/B (DCD)



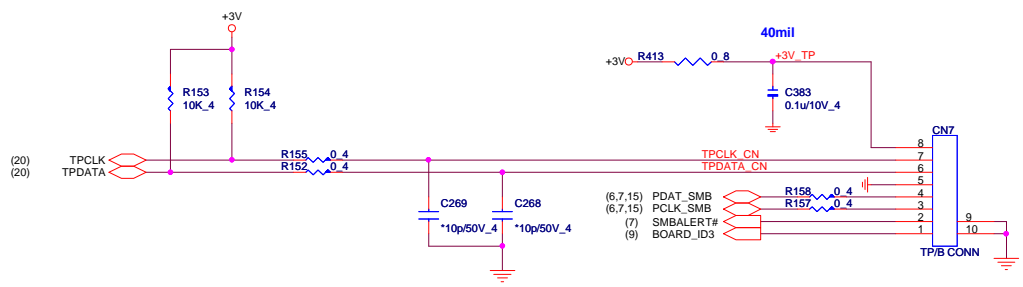
# KEYBOARD (KBC)



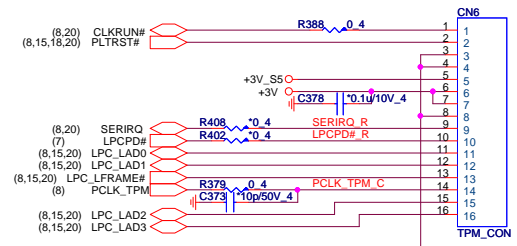
# CPU FAN CTRL (THM)



# TOUCH PAD (TPD)



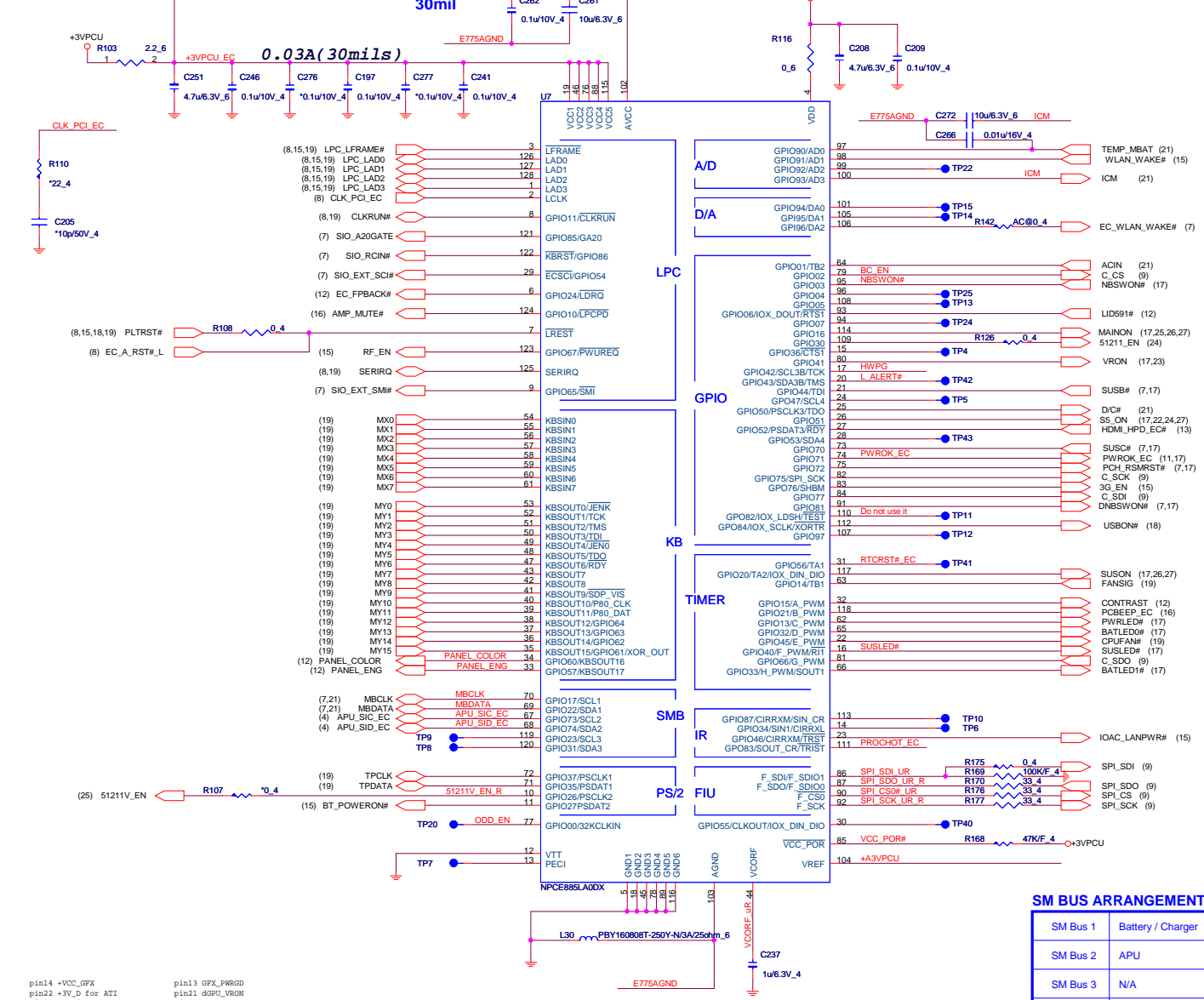
# TPM (TPM)



**Quanta Computer Inc.**  
PROJECT : ZHG

|       |                                     |                |
|-------|-------------------------------------|----------------|
| Size  | Document Number                     | Rev            |
|       | <b>KB/BT/TP/LED/Power Connector</b> | 1A             |
| Date: | Tuesday, January 10, 2012           | Sheet 19 of 28 |

**EC(KBC)**

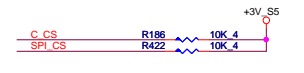


**SM BUS ARRANGEMENT TABLE**

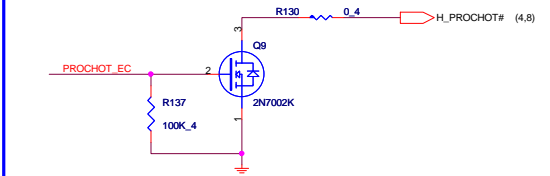
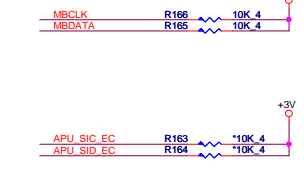
| SM Bus 1 | Battery / Charger |
|----------|-------------------|
| SM Bus 2 | APU               |
| SM Bus 3 | N/A               |
| SM Bus 4 | N/A               |

pin14 +VCC GFX      pin13 GFX\_PWRGD  
 pin22 +3V\_D for ATI      pin21 dGPU\_VRON  
 pin24 +1V for ATI      pin23 +VGPU\_CORE  
 pin26 +1.8V\_GPU for ATI      pin25 +1.5V\_GPU  
 pin28 GPU\_RST#      pin27 dGPU\_PWROK

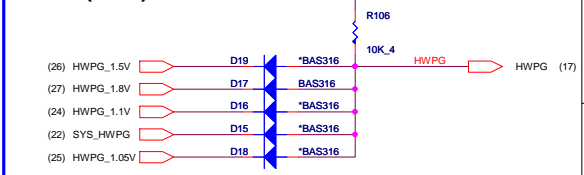
**SPI PU(KBC)**



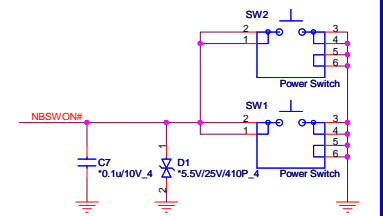
**SM BUS PU(KBC)**

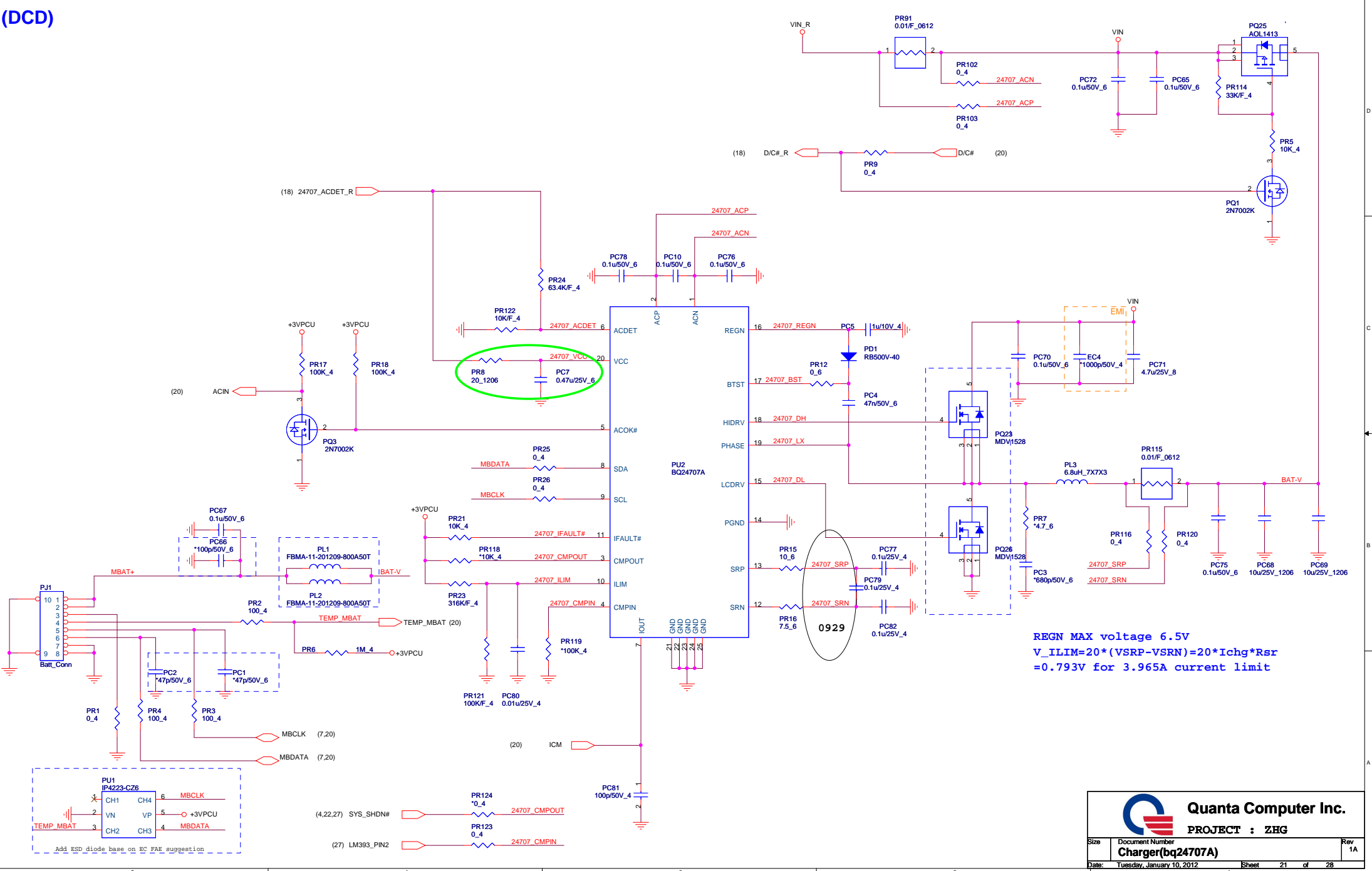


**HWPG(KBC)**




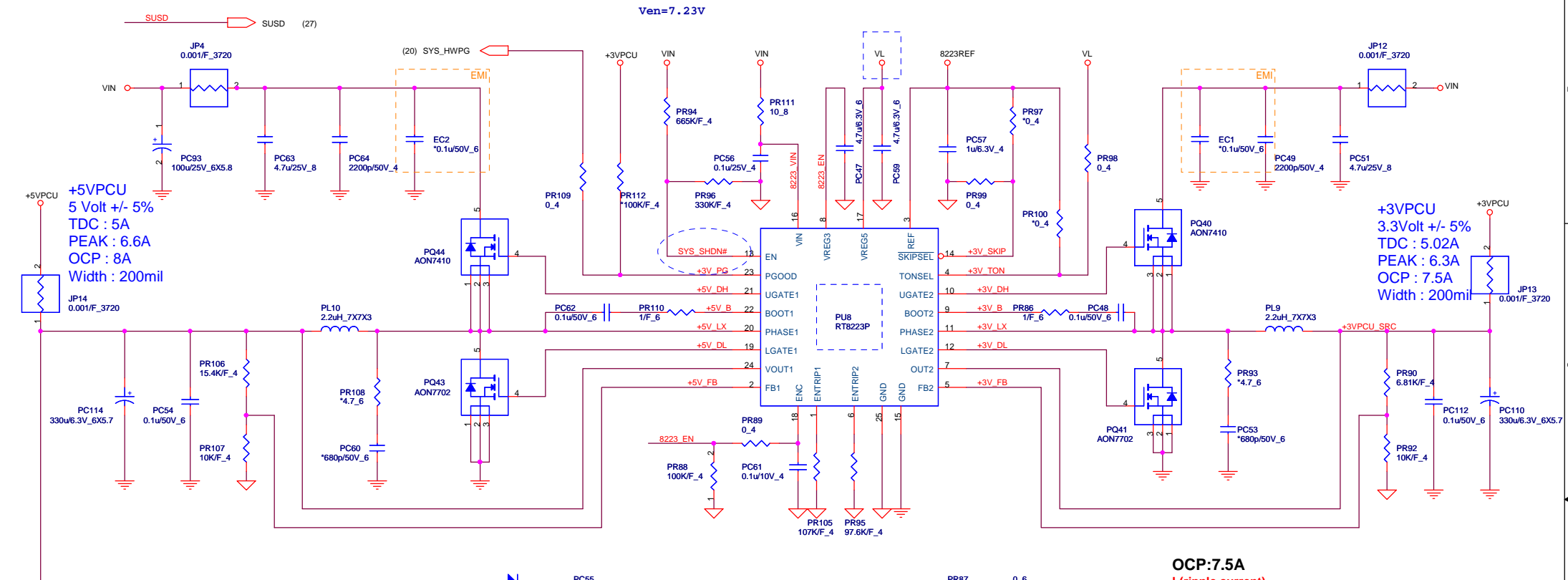
**POWER-ON SWITCH (UIF)**





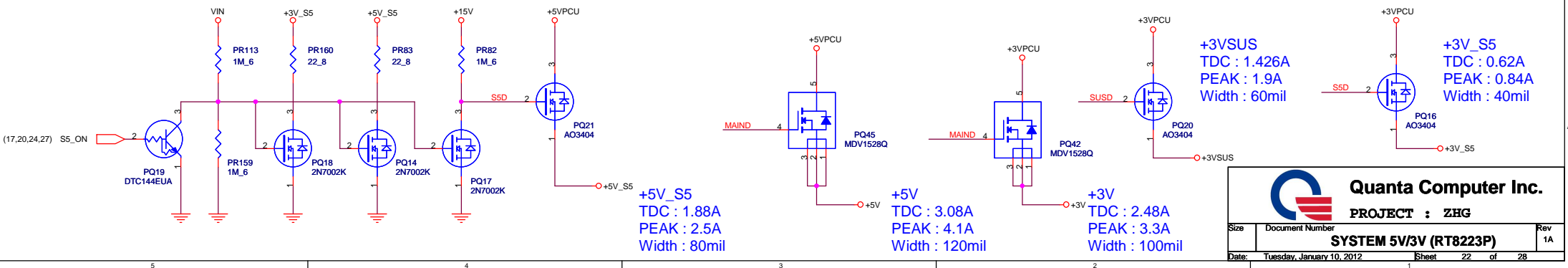
REGN MAX voltage 6.5V  
 $V_{ILIM} = 20 * (V_{SRP} - V_{SRN}) = 20 * I_{chg} * R_{sr} = 0.793V$  for 3.965A current limit

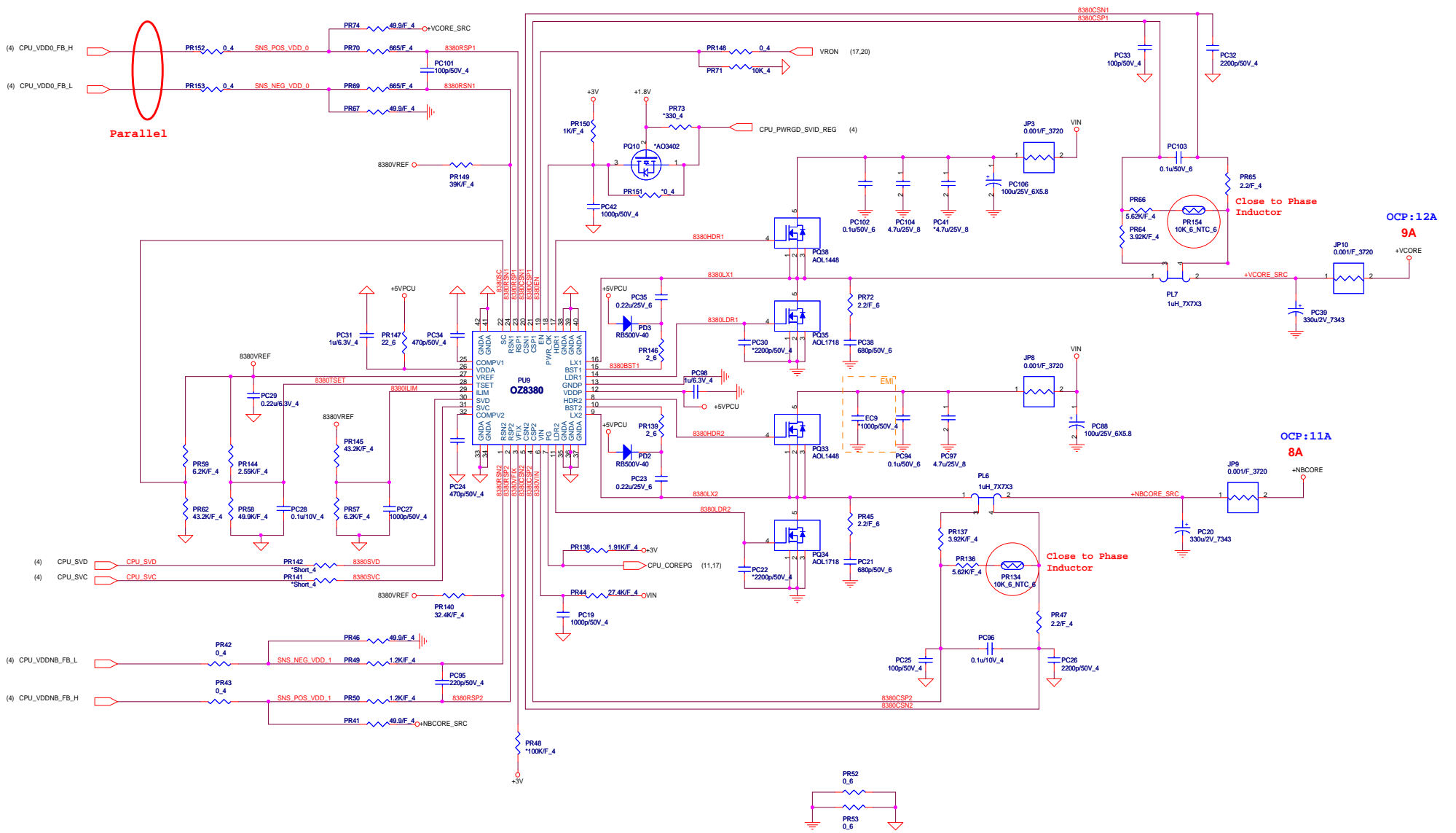
|   |                           |                |
|---|---------------------------|----------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : ZHG</b> |                           |                |
| Size  | Document Number           | Rev            |
|   | <b>Charger(bq24707A)</b>  | 1A             |
| Date:   | Tuesday, January 10, 2012 | Sheet 21 of 28 |



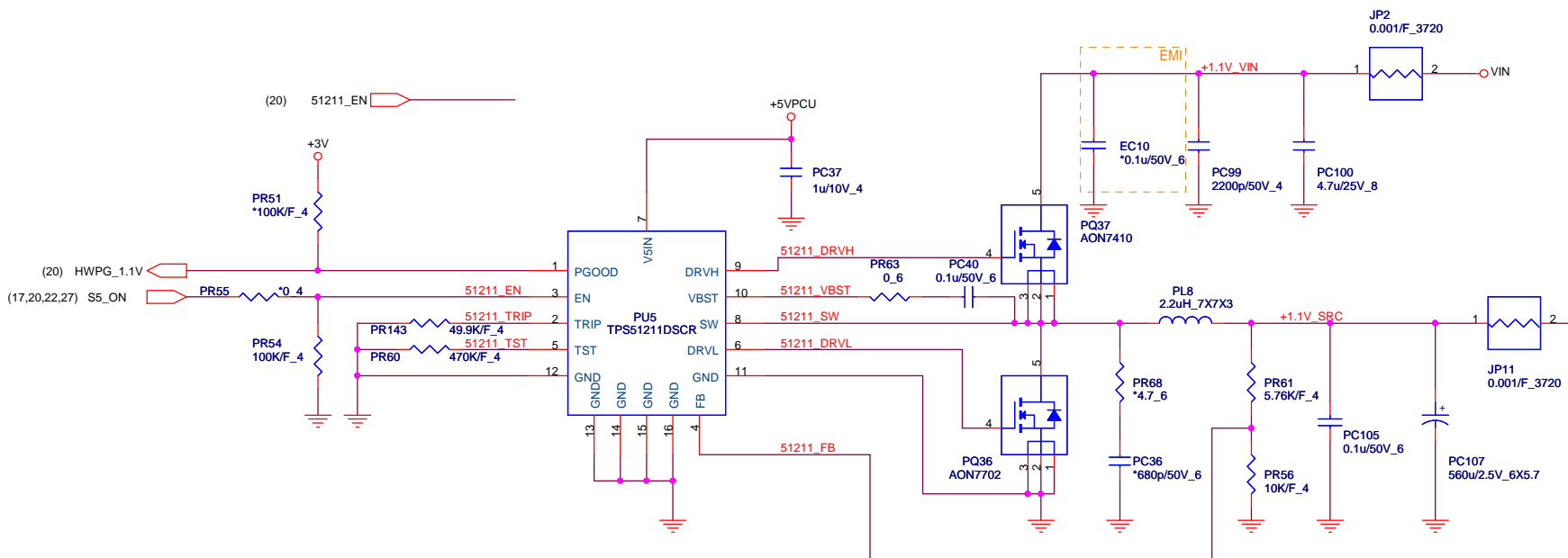
**OCP:8A**  
L(ripple current)  
=(9-5)\*5/(2.2u\*0.4M\*9)  
=2.525A  
Iocp=8-(2.525/2)=6.74A  
Vth=6.74A\*14mOhm=94.32mV  
R(Ilim)=(94.32mV\*10)/10uA  
=94.32K

**OCP:7.5A**  
L(ripple current)  
=(9-3.3)\*3.3/(2.2u\*0.5M\*9)  
~1.9A  
Iocp=7.5-(1.9/2)=6.55A  
Vth=6.55A\*14mOhm=91.7mV  
R(Ilim)=(91.7mV\*10)/10uA  
~91K



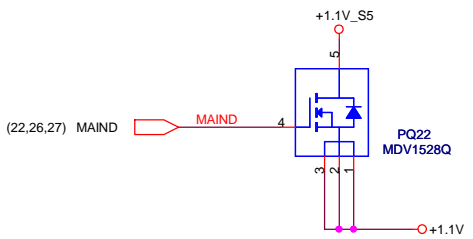


(DCD)




**+1.1V\_S5**  
 1.1 Volt +/- 5%  
 TDC : 3A  
 PEAK : 4A  
 OCP : 5A  
 Width : 120mil

OCP=5A  
 L ripple current  
 $= (19-1.1) * 1.1 / (2.2 * 290k * 19)$   
 $= 1.624A$   
 $V_{trip} = 5 - (1.624 / 2) * 14mohm$   
 $= 0.058629V$   
 $R_{limit} = 0.058629 / 10uA * 8 = 46.9Kohm$

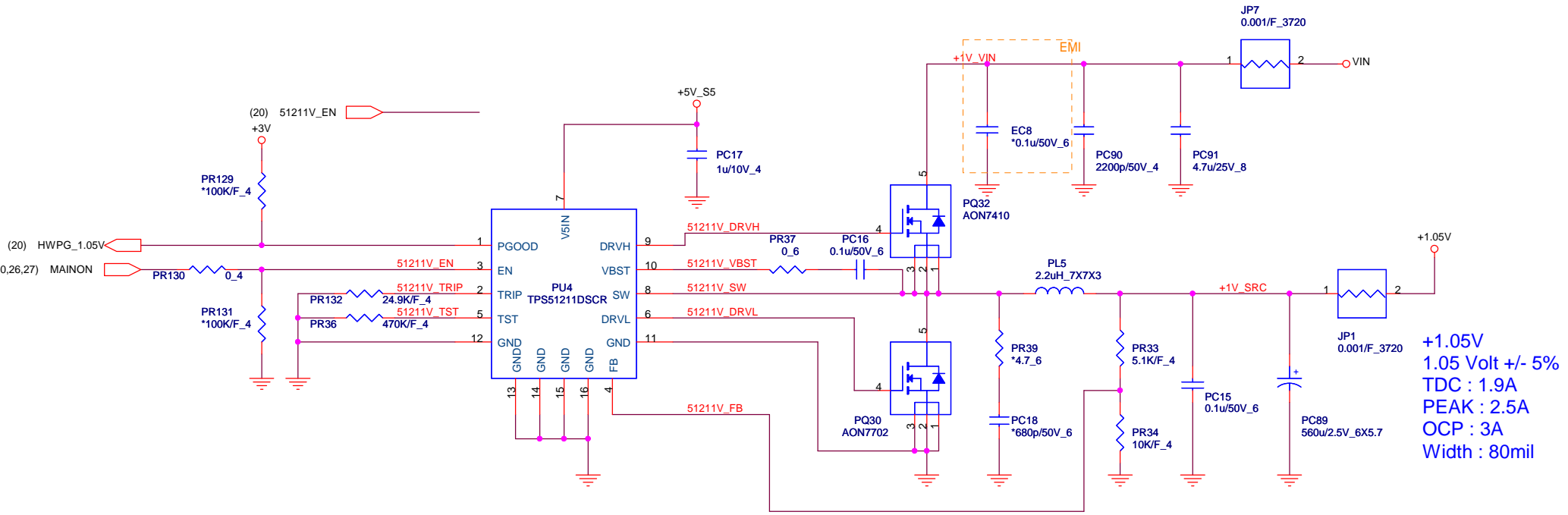


**+1.1V**  
 TDC : 2.73A  
 PEAK : 3.64A  
 Width : 120mil

|  |  |           |
|--|--|-----------|
|  <b>Quanta Computer Inc.</b><br>PROJECT : ZHG |  | Rev<br>1A |
|  |  |           |
| Date: Wednesday, January 11, 2012 Sheet 24 of 28   |  |           |




# (DCD)

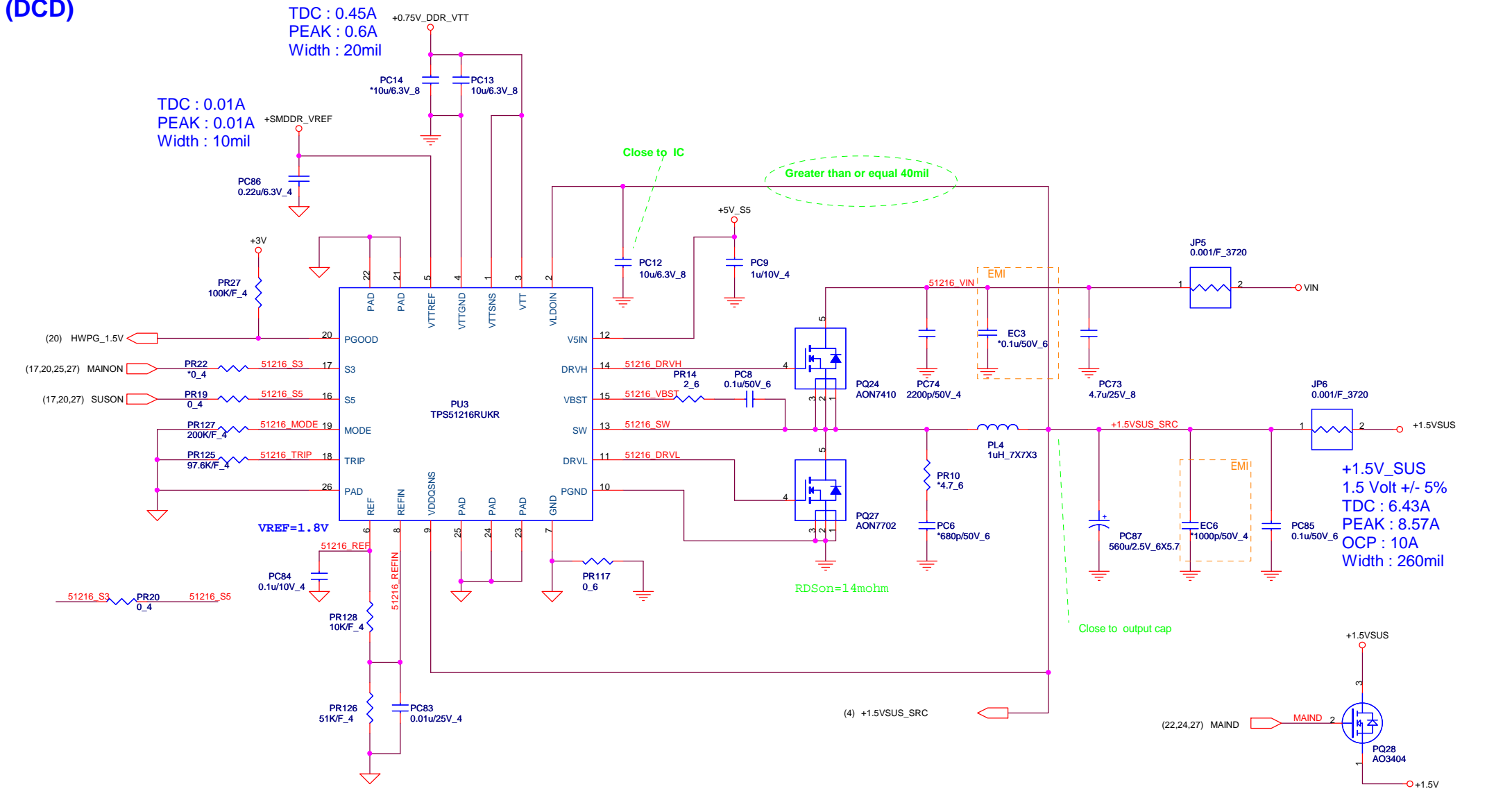


**+1.05V**  
 1.05 Volt +/- 5%  
 TDC : 1.9A  
 PEAK : 2.5A  
 OCP : 3A  
 Width : 80mil

OCP=3A  
 $L$  ripple current  
 $= (19 - 1.05) * 1.05 / (2.2u * 290k * 19)$   
 $= 1.555A$   
 $V_{trip} = 3 - (1.555 / 2) * 14mohm$   
 $= 0.03111V$   
 $R_{limit} = 0.03111 / 10uA * 8 = 24.89Kohm$

|   |                             |                |
|---|-----------------------------|----------------|
|  <b>Quanta Computer Inc.</b><br><b>PROJECT : ZHG</b> |                             | Rev            |
|   |                             | 1A             |
| Size  | Document Number             |                |
| <b>+1.05V(TPS51211)</b>   |                             |                |
| Date:   | Wednesday, January 11, 2012 | Sheet 25 of 28 |

(DCD)



TDC : 0.01A  
PEAK : 0.01A  
Width : 10mil

TDC : 0.45A  
PEAK : 0.6A  
Width : 20mil

+1.5V\_SUS  
1.5 Volt +/- 5%  
TDC : 6.43A  
PEAK : 8.57A  
OCP : 10A  
Width : 260mil

OCP=10A  
I ripple current  
= (19-1.5)\*1.5/(1u\*400k\*19)  
= 3.454A  
Vtrip=10-(3.454/2)\*14mohm  
= 0.1158V  
Rlimit=0.1158/10uA\*8=92.657Kohm

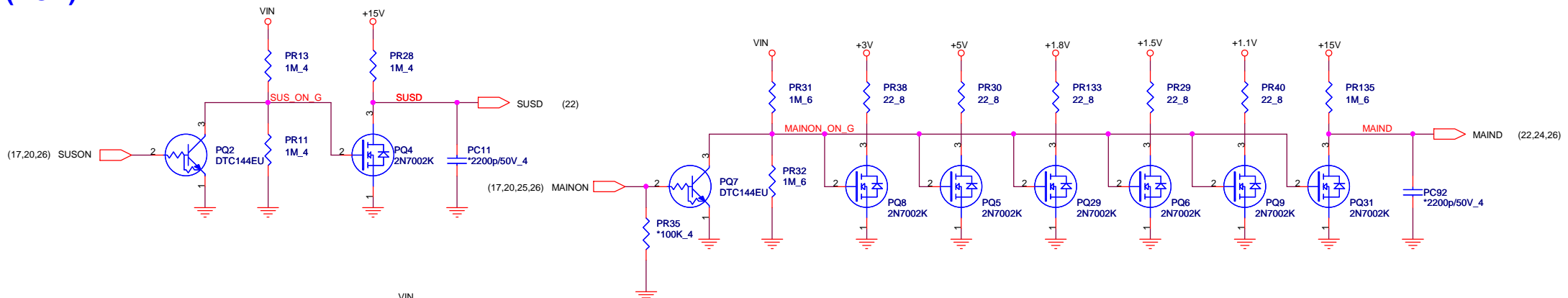
|                 | S3 | S5 | +1.5VSUS | REF | VTT |
|-----------------|----|----|----------|-----|-----|
| S0              | 1  | 1  | ON       | ON  | ON  |
| S3 (mainon off) | 0  | 1  | ON       | ON  | OFF |
| S4/S5           | 0  | 0  | OFF      | OFF | OFF |

**Quanta Computer Inc.**  
PROJECT : ZHG

Size Document Number Rev  
**DDR 1.5V(TPS51216)** 1A

Date: Tuesday, January 10, 2012 Sheet 26 of 28

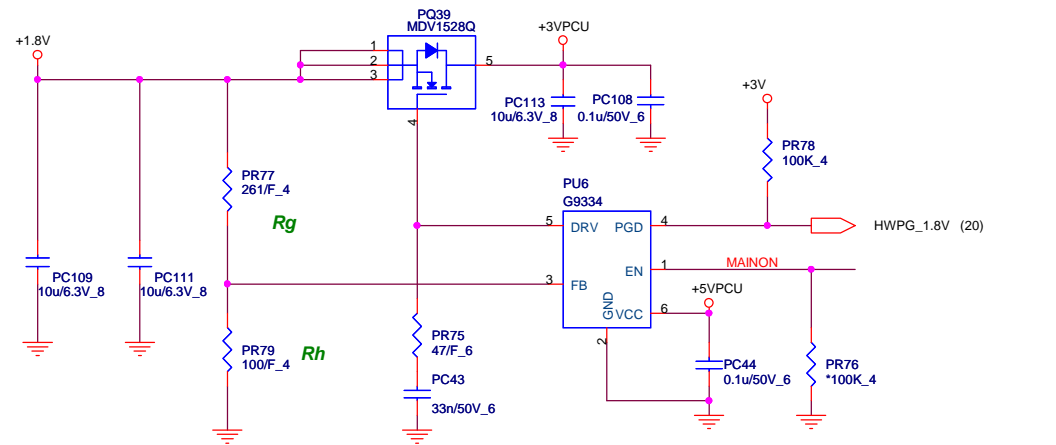
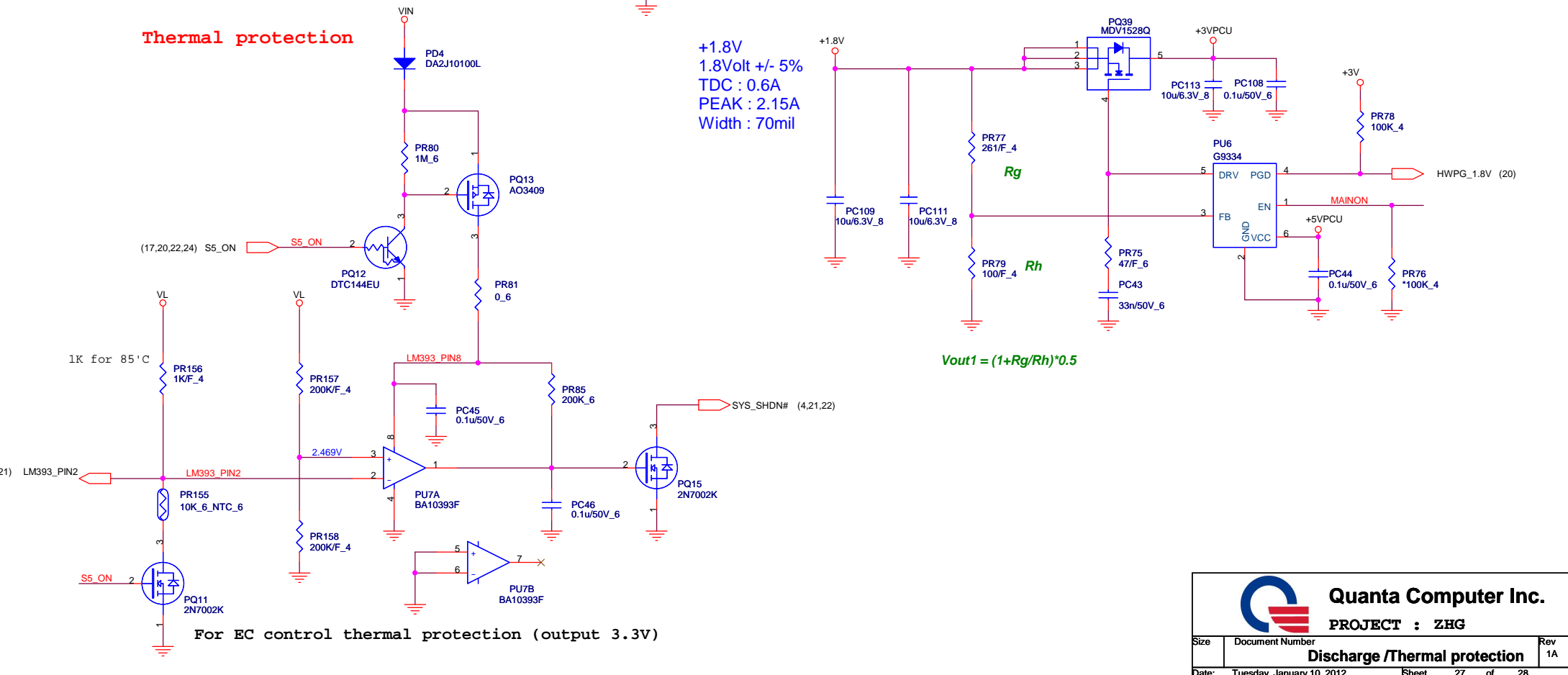
(DCD)



Thermal protection

+1.8V  
 1.8Volt +/- 5%  
 TDC : 0.6A  
 PEAK : 2.15A  
 Width : 70mil

$V_{out1} = (1 + R_g/R_h) * 0.5$




|   |  |                |
|---|--|----------------|
| <p><b>Quanta Computer Inc.</b></p> <p>PROJECT : ZHG</p> |  | Rev<br>1A      |
|   |  |                |
| Date: Tuesday, January 10, 2012                         |  | Sheet 27 of 28 |

| MODEL | REV | CHANGE LIST |  |
|-------|-----|-------------|--|
|-------|-----|-------------|--|

| Page | ZHG MB BOARD |    |
|------|--------------|----|
|      | From         | To |
| 1    | 1A           |    |
| 2    | 1A           |    |
| 3    | 1A           |    |
| 4    | 1A           |    |
| 5    | 1A           |    |
| 6    | 1A           |    |
| 7    | 1A           |    |
| 8    | 1A           |    |
| 9    | 1A           |    |
| 10   | 1A           |    |
| 11   | 1A           |    |
| 12   | 1A           |    |
| 13   | 1A           |    |
| 14   | 1A           |    |
| 15   | 1A           |    |
| 16   | 1A           |    |
| 17   | 1A           |    |
| 18   | 1A           |    |
| 19   | 1A           |    |
| 20   | 1A           |    |
| 21   | 1A           |    |
| 22   | 1A           |    |
| 23   | 1A           |    |
| 24   | 1A           |    |
| 25   | 1A           |    |
| 26   | 1A           |    |
| 27   | 1A           |    |
| 28   | 1A           |    |
| 29   |              |    |
| 30   |              |    |
| 31   |              |    |
| 32   |              |    |
| 33   |              |    |
| 34   |              |    |
| 35   |              |    |
| 36   |              |    |
| 37   |              |    |
| 38   |              |    |
| 39   |              |    |
| 40   |              |    |
| 41   |              |    |

| ZHG M/B | REV | First Release   |
|---------|-----|---|
|         | A   |   |
|         | B   | <p>Add R3439<br/>Del R237,R204,R222<br/>Change CN3016,CN3017,CN3018 footprint and PN<br/>Change PC101,PC104 PN</p> <p>Change CN3015,CN3006,CN3004 footprint<br/>SWAP RP9,RP10<br/>Add R3440,R3441,R3442,C6239,C6240,C6241<br/>Del TP53,TP15,TP14,TP24<br/>Change PR20 PN and footprint,PR12 PN<br/>Add R3443,R3444,R3446,R3445<br/>Update CN16,CN3011 PN</p> <p>Update CN16,CN3011 footprint<br/>Change PC73,PC79,PC80,PC82,PC83,PC90 footprint<br/>Swap CP3001,CP3002,CP3003,CP3004,CP3005,CP3006 pin<br/>Change CN3001 PN and footprint.<br/>Delete R3031,C3036,C3021<br/>Delete C3057,C3064,C3062,C3060,C3056,C3061<br/>Add R3447,R3448<br/>Delete TP21,TP11</p> <p>Add R3449 and change CN3008 PN and footprint<br/>Swap CN3001,RP8<br/>Change CN3017,CN3016 PN<br/>Delete R113,R125</p> <p>Change R3289 to 0ohm<br/>Swap Q3030 pin define<br/>PU Board_ID3 and Board_ID2, modify CN3008 net<br/>Delete R3009<br/>Change C3013 to 1uF<br/>Add R3450,R3451<br/>Change CN3003 pin define</p> <p>Swap L3026<br/>Change R142 to 100K<br/>Delete R3435,C3260. Change CN3008 PN and footprint<br/>Delete R3272,Q3019,R3256,R3270,TP18,TP25,TP28<br/>and add Q3036,Q3035,R3452<br/>Add PQ45,PR162,SW2,R3453,RP11,D3022<br/>Delete R3438<br/>Unstaff D10,D54,D55,R242,R206 and staff R369,R223,Q3033,RN3001</p> <p>Modify CN3003 and U4 pin define<br/>Add Q3037<br/>Unify the value, function code, P/N, description</p> |
|         | C   | <p>Delete T6,T15,R215,R202,Q12,R3425,R3426<br/>Add R3454,PQ46,C6242<br/>Add HOLE<br/>Update CN3015 PN<br/>Change CN3008 pin define<br/>Change CN3006 footprint<br/>Add R3460,C6243,R3457,R3459,R3455,<br/>R3456,Q3038,R3458,R3461 and reserve IOAC function</p> <p>Change Y3 footprint and staff R371<br/>Update U17,CN3015,CN14,CN3001 P/N<br/>Change CN3006 footprint<br/>Add R3462,Q3039<br/>Delete R163,RT1,R3459<br/>Add L3029~L3035,R3463~3476 for EMI<br/>Unstaff C418<br/>Staff R3418,R3200,R3434,R3439<br/>Change CN3008 PN and footprint</p> <p>Staff R115<br/>Delete CN3007 power trace for layout<br/>Add PQ47,PQ48,PR163,PR165,PR164,PC118<br/>Delete TP29 and add net 1.1V_S5_EN<br/>Add R3477,R3478</p> <p>Modify LVDS common choke pin define<br/>Add TP63~TP70 for layout<br/>Remove G2,G3 and add T3051,T3052<br/>Change Y3,C3041 footprint<br/>Modify PU2 pin define</p> <p>Change PR3,PR20,PR12,PC11 PN<br/>Add EC1~EC10 for RF<br/>Add EC11~EC18 for EMI<br/>Add R3479 and C6244,R3480,R3481<br/>Delete EC7,EC8,EC10,EC4,PAD3</p> <p>Staff PR154,R3480 and unstaff PR149<br/>Staff R206 and unstaff R223</p>   |

|                            |                        |                        |                   |
|----------------------------|------------------------|------------------------|-------------------|
| ZHG                        | PCBA NO : 31ZHGM0000   | REV: A                 | DOC. NO : 206     |
| APPROVED BY : Edison Huang | CHECK BY : Kevin Hsieh | DRAWING BY : Benson Yo | DATE : 2012/01/10 |



**Quanta Computer Inc.**  
PROJECT : ZHG

Size Document Number Rev  
**CHANGE LIST** 1A

Date: Tuesday, January 10, 2012 Sheet 28 of 28